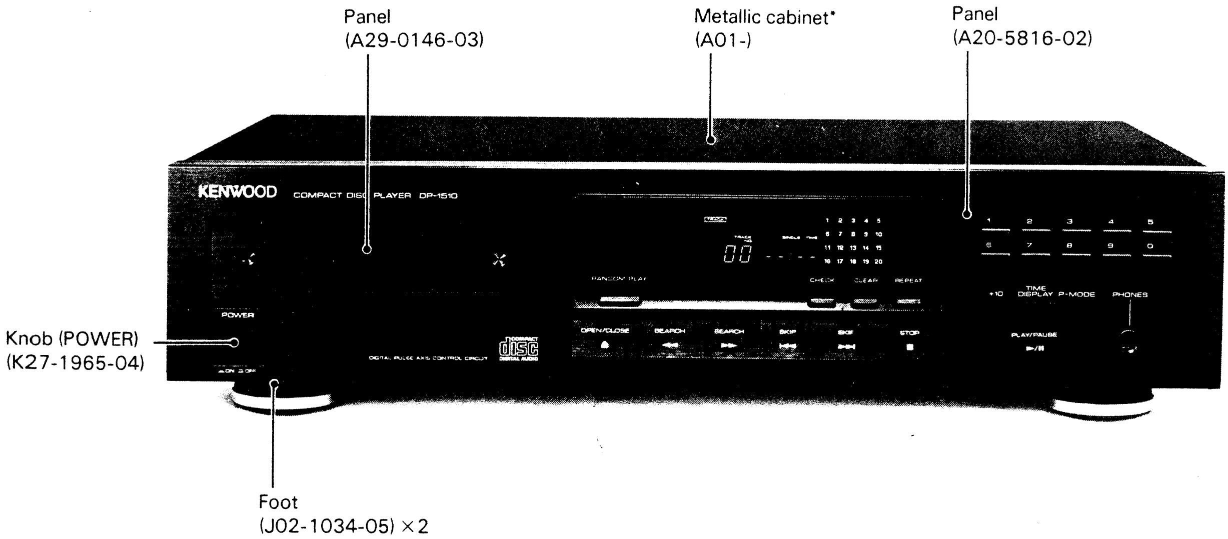
COMPACT DISC PLAYER

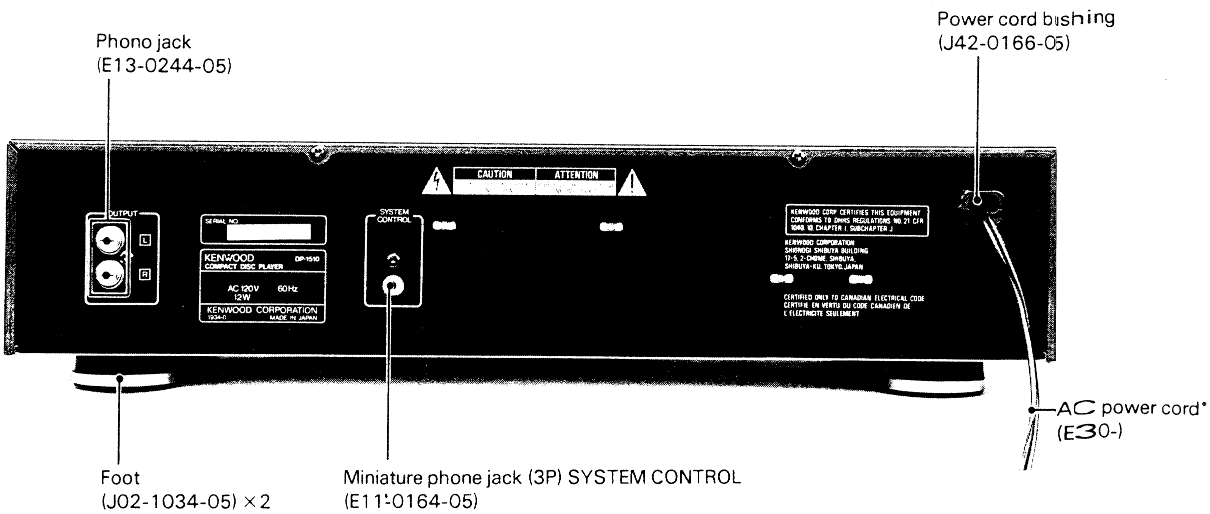
DP-1510

SERVICE MANUAL

KENWOOD

B51-3804-00(B)2971





J: Japan made
S: Singapore made

In complicance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

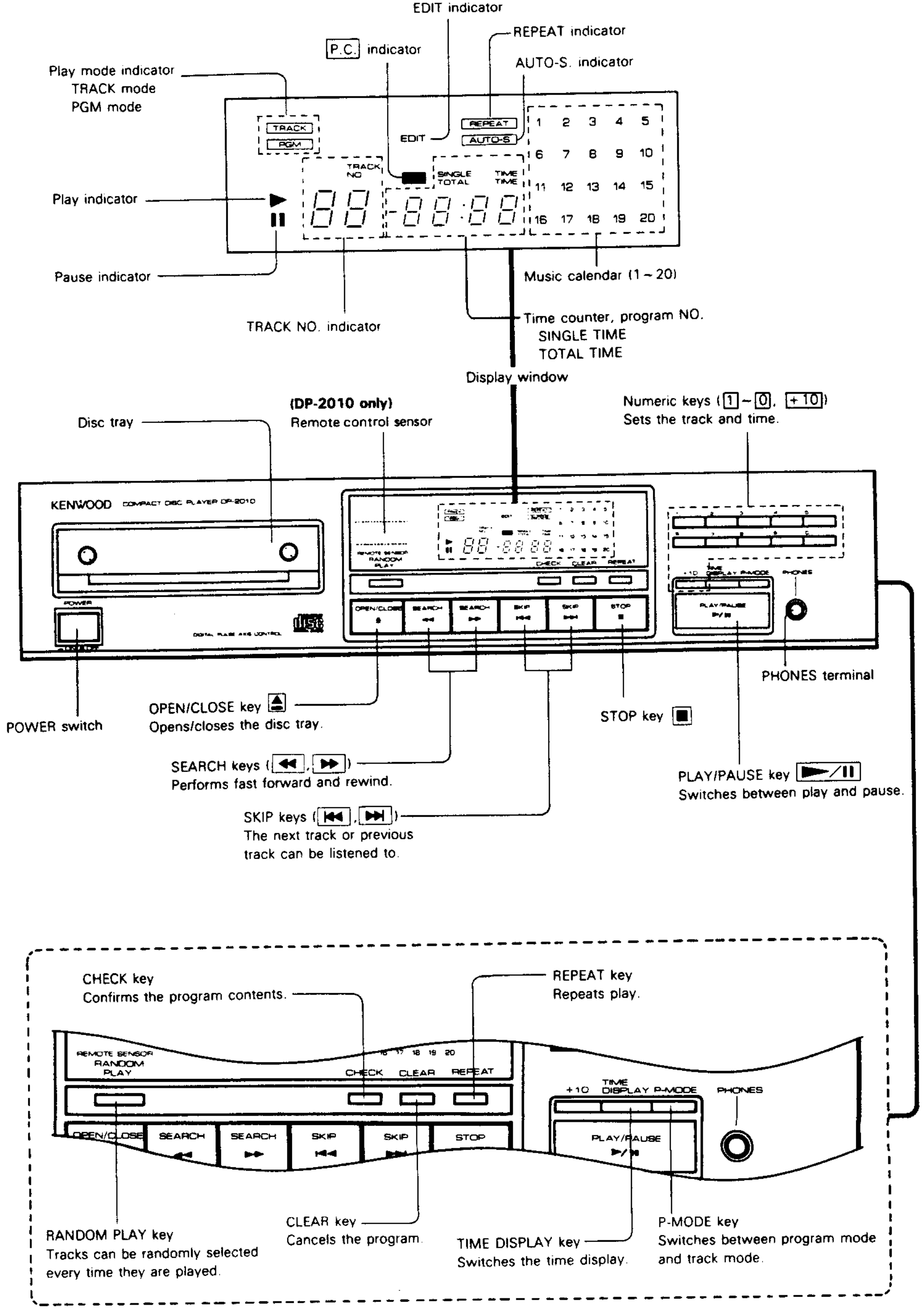
Caution:
The Mechanism ass'y used with the DP-1510 varies in two types depending on the manufacturing location. (Japan, Singapore)

*** Refer to parts list on page 114.**

CONTENTS

Caution:
The Mechanism ass'y used with the DP-1510 varies in two types depending on the manufacturing location. (Japan, Singapore)

CONTROLS AND INDICATORS



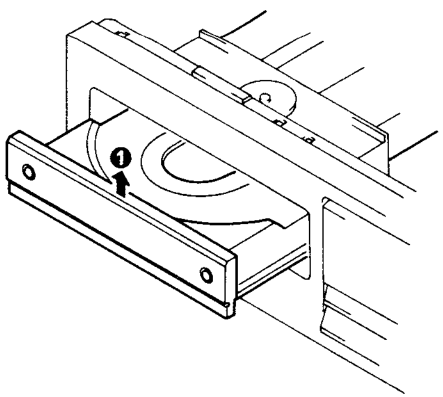
DISASSEMBLY FOR REPAIR
JAPAN MADE

JAPAN MADE

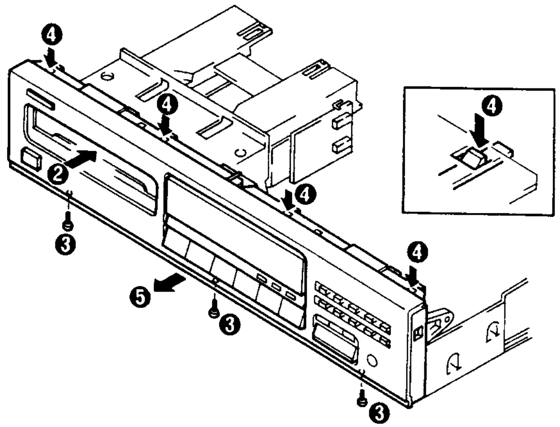
1. Removing the Control Unit

- Remove the case beforehand. There is no need to remove the stand-offs or holder.

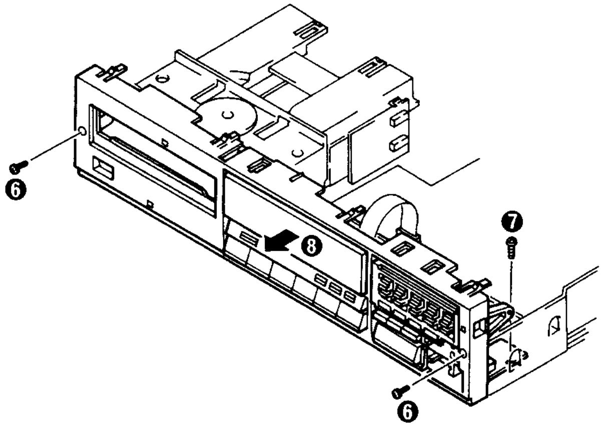
1) Remove the tray panel by sliding it upward ❶.



2) Push tray in the direction of ❷
3) Remove the three screws ❸, unlatch the four hooks ❹ and remove the front panel ❺



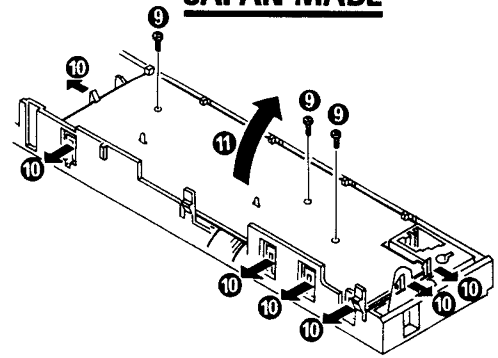
4) Remove the two screws ❻ and the headphone board screw ❼ to remove the sub-panel ❽



DISASSEMBLY FOR REPAIR
JAPAN MADE

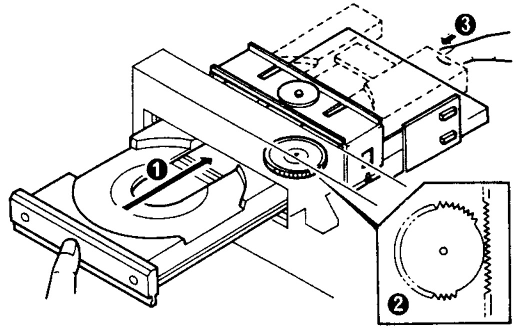
JAPAN MADE

5) Remove the three screws ❾, unlatch the seven hooks ❿ and remove the control unit ⓫

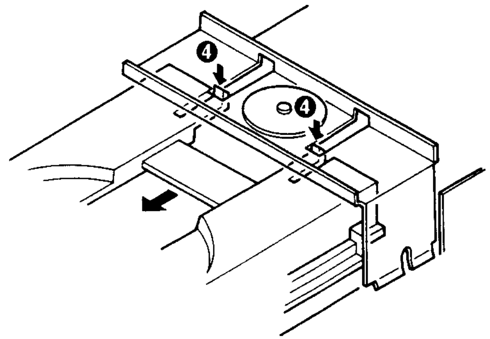


2. Removing the Tray

1) First open the tray and switch power off.
2) Slowly push the tray inwards ❶1. There will be a point where the gear will be at a point where it will be free ❷.
3) Push the tray toward yourself while pushing outward from the back ❸.

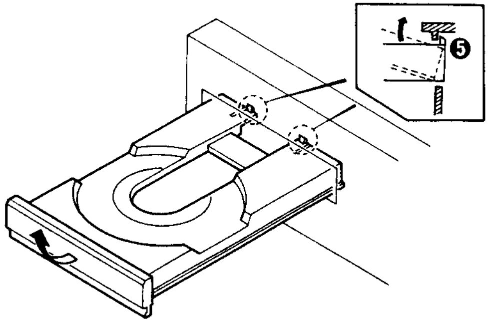


4) Unlatch the two stopper hooks ❹.



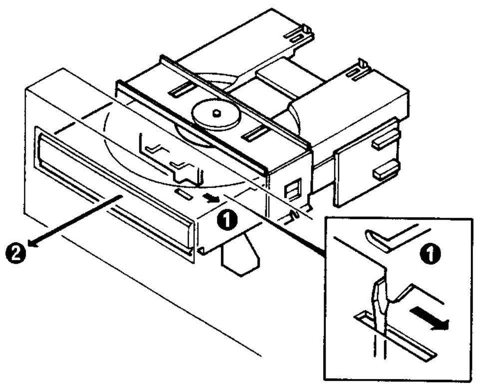
DISASSEMBLY FOR REPAIR
JAPAN MADE

5) When removing the tray, the stopper hooks will latch onto the sub-unit. Remove by tilting the tray upward as in ❺.



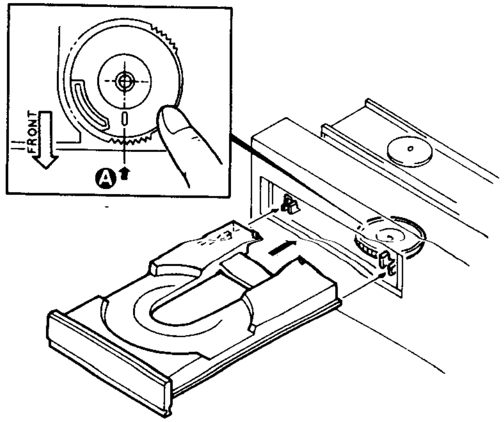
2-1. When there is no power, or the tray does not come out even if OPEN is pressed.

1) Insert a screw driver through the slit in the bottom plate and push the lever forward ❶.
2) The tray will move forward a little and the gear will be freed so the tray can be pulled out ❷.



3. Replacing the tray

1) Move the gear into the same position as A .
2) Push the tray in on the guides on both sides of the slot.
3) Turn on the power and switch MD Assy to UP.
4) Push the tray OPEN/CLOSE KEY to confirm normal movement.

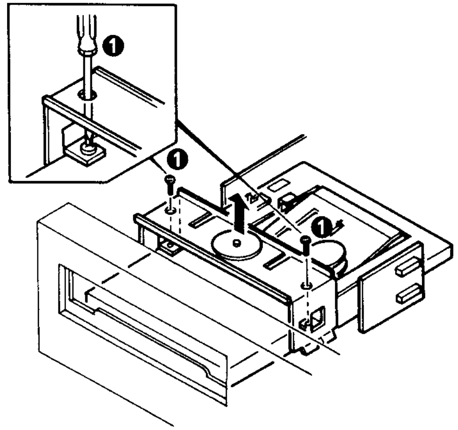


DISASSEMBLY FOR REPAIR
JAPAN MADE

4. Removing the Pick-up

- Remove tray beforehand.

1) Remove the two screws ❶ and take off the metal clamp.



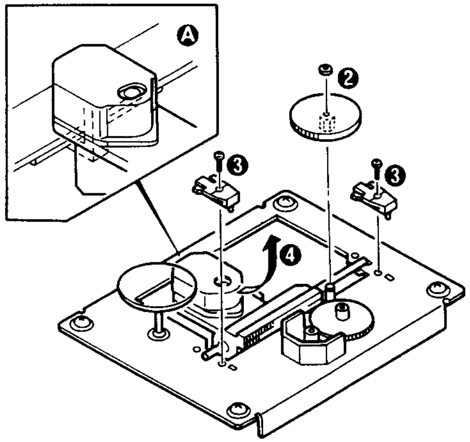
2) Remove the gear after taking off the ring stopper ❷.
3) Romove the two clamps ❸.
4) Remove the Pick-up as shown in the diagram ❹.

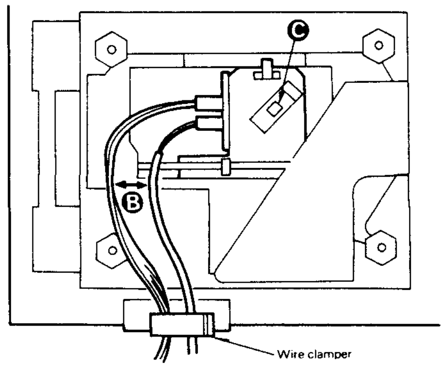
Note 1) Replacement of the Pick-up

- **Make sure that clamp and the guide of the Pick-up meet A .**
- **Keep the two cords coming out of the Pick-up as far away from eachother as possible B .**

Note 2) When changing the Pick-up

- **To protect the Laser Diode (LD) of the service part Pick-up (J91-0385-08), the LD shortland C is shorted with solder. When changing this part, remove the solder only after the connector has been connected.**





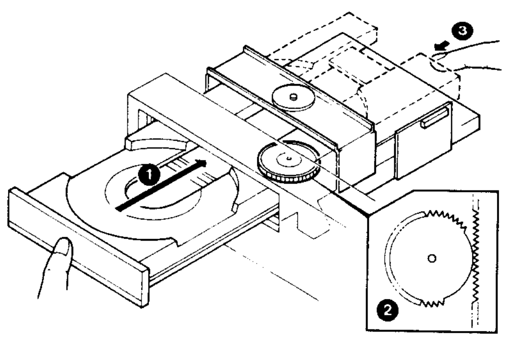
DISASSEMBLY FOR REPAIR
SINGAPORE MADE

1. Removing and Installing the Tray

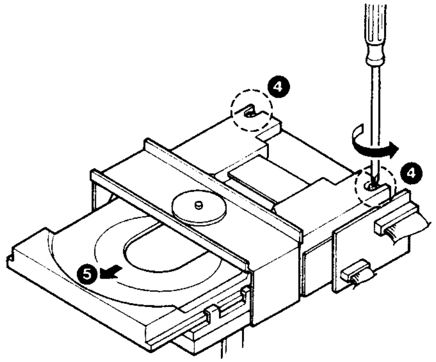
1–1. Removing the Tray

- Open the disc tray and turn the power OFF.

1. Push the tray gradually into the unit (1) by your hand. In this condition, the gear will be released (2).
2. Push the rear end of the tray toward the front to remove the tray until it stops (3).

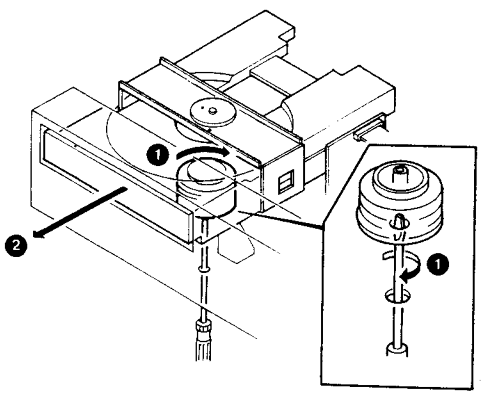


3. Remove the two screws (4) of the tray stopper.
4. Draw out the tray (5).



Note : When the power can not be turned ON, or when the tray can not be opened by pressing the OPEN key :

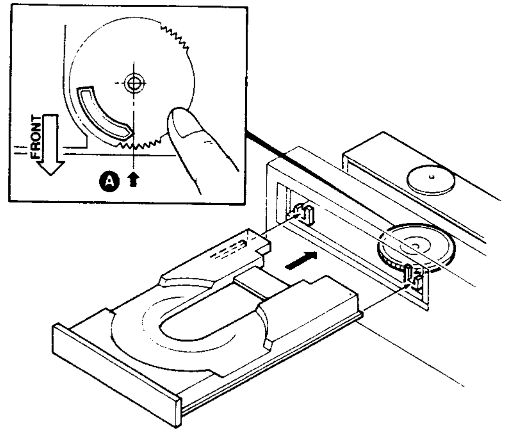
1) Rotate the control cam by a screwdriver, etc. set into the hole on the bottom plate of the unit as shown (1).
2) When the tray is comes out slightly, the gear is released. Then take out the tray toward the front (2).



DISASSEMBLY FOR REPAIR
SINGAPORE MADE

1–2. Installing the Tray

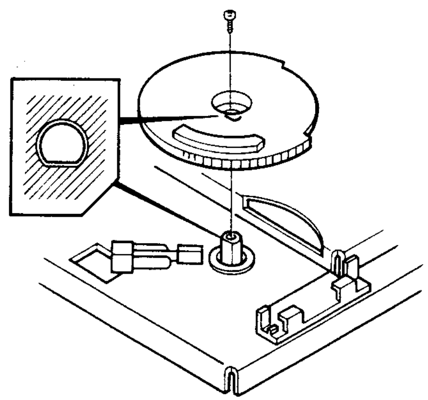
1. Set the gear to the position (A) shown in the diagram.
2. Insert the tray along with the guide rails on the both sides.



2. Installing the Loading Gear

2–1. Installing the Drive Gear

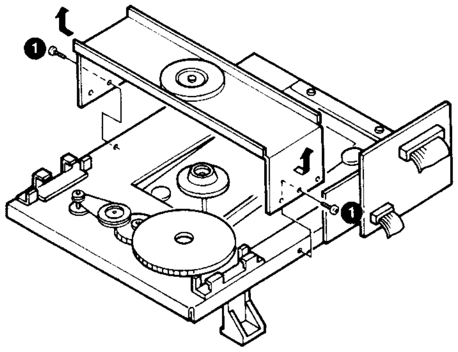
Align the drive gear with the cutout section of the control cam to install it.



DISASSEMBLY FOR REPAIR
SINGAPORE MADE

3. Removing the Pickup

* Remove the tray.
1. Remove the two screws (1) and remove the catch of the clamper.



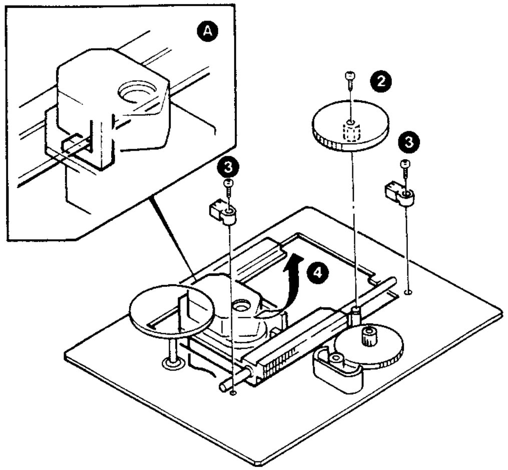
2. Remove one screw and take out the gear (2).
3. Remove the two shaft clamper (3).
4. Remove the pickup in the direction of the arrow (4).

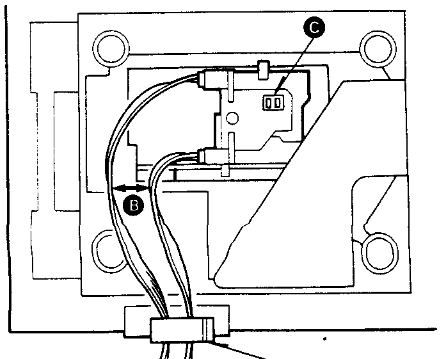
Note 1 : When installing the pickup :

- o Install the pickup so that the metal fittings are engaged with the guide of the pickup (A).
- o Keep the flat cable from the pickup away from the unit as far as possible (B).

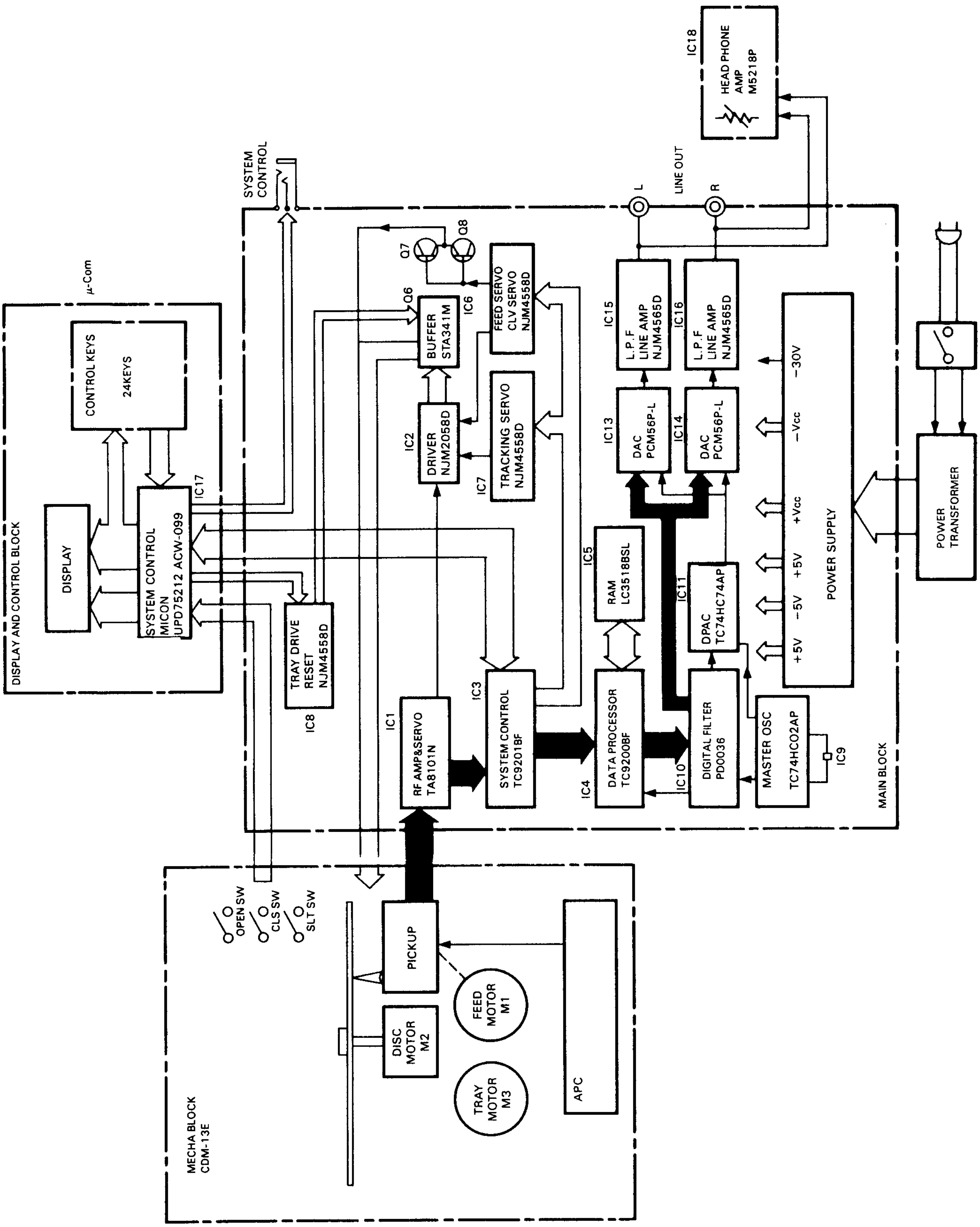
Note 2 : When the pickup has been replaced :

- o For the protection of the laser diode (LD), the LD short land of the pickup may be shorted. If so, after connecting the connector, unsolder the short land (C).





BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1. Component Functions

1-1. Control Circuit Unit (X29-1990-00)

Components	Part No.	Use/Function	Operation/Condition/Interchangeability
IC1	M5223P	OP AMP	Deviation Amplifier of the ALPC circuit
Q1	2SC3246	Transistor	Constant Current/Voltage Ripple Filter for +5 V of the ALPC circuit
Q2	2SC945 (A) (Q, C) 2SC1740S (Q, R)	Transistor	Constant Current/Voltage Deviation amplifier for +5 V of the APLC circuit
Q3	2SA733 (A) (Q, P) 2SA933S (Q, R)	Transistor	Constant Current/Voltage Ripple Filter for −5 V of the APLC circuit
Q4	2SA733 (A) (Q, P) 2SA933S (Q, R)	Transistor	ON/OFF Control Switch of the Laser of the APLC circuit (When LDON is "L" then OFF, and when "H" then ON)
Q5	2SA733 (A) (Q, P) 2SA933S (Q, R)	Transistor	Laser drive transistor of the APLC circuit

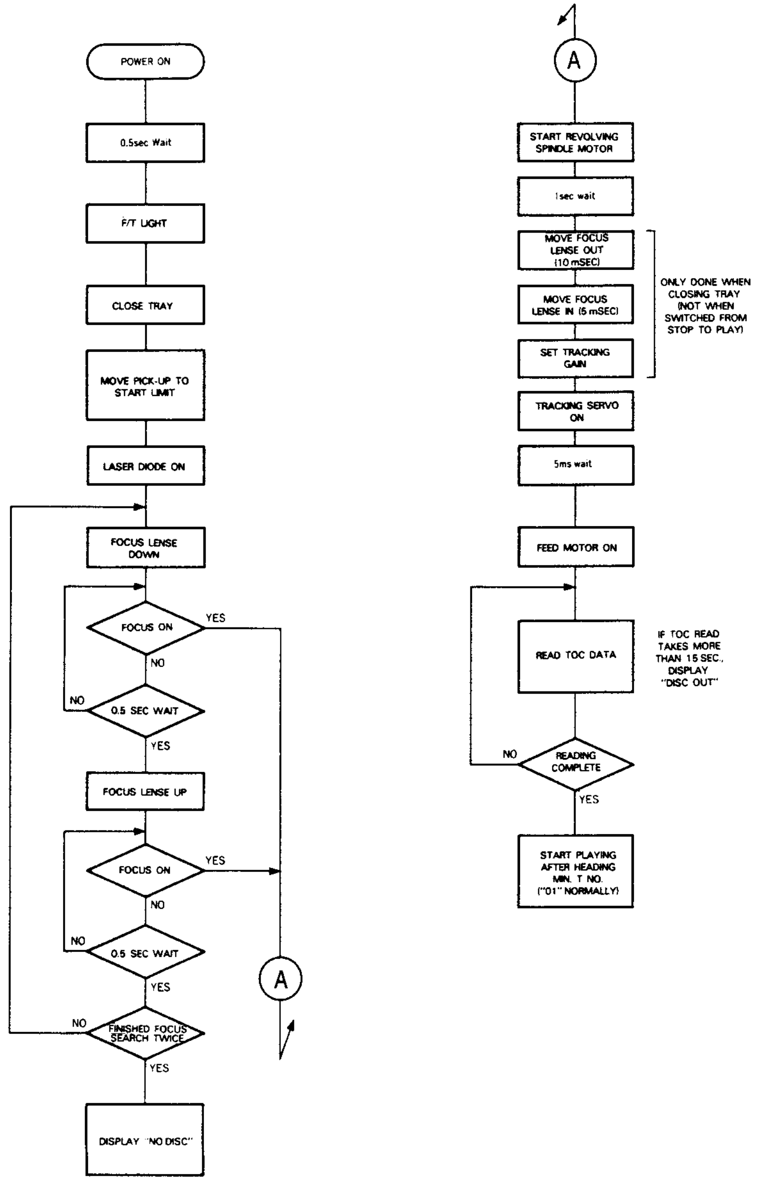
1-2. CD Player Unit (X32-1400-10)

Components	Part No.	Use/Function	Operation/Condition/Interchangeability
IC1	TA8101N	RF Servo IC	Producing of and Data Slicing of the Focus Area AMP, Tracking Area AMP, and RF Sub-beam Signal AMP for the EFMI Summing Signal
IC2	NJM2058D	OP AMP	OP AMP for (1/4) V_{REF} (2/4) Focus Coil Drive (3/4) Tracking Coil Drive (4/4) Feed Motor Drive
IC3	TC9201BF	Servoprocessor	CLV Control of the Feed Servo, Search Control and Disc Motor
IC4	TC9200BF	LSI Digital Signal Processor	LSI for Synchronizing Isolation, EFM Signal Demodulator, Error Detector, Correction Processor
IC5	LC3518BSL-15	S-RAM	16K RAM for Signal Processing
IC6	NJM4558D	OP AMP	(1/2) Tracking Coil Drive (2/2) Disc Motor Drive
IC7	NJM4558D	OP AMP	(1/2) Tracking Coil Drive (2/2) Feed Motor Drive
IC8	NJM4558D	OP AMP	(1/2) Tray Motor Drive (2/2) OP AMP for Producing the Reset Signal
IC9	TC74HCO2AP	NOR GATE	(1/4) Inverter for the LRCK Signal (2/4) Inverter for 16.9344 MHz (3/4) Inverter for Bit Clock (4/4) Inverter for Bit Clock
IC10	PD0036	Digital Filter	Eight Times Over Sampling Digital Filter
IC11	TC74HC74AP	FLIP/FLOP	D FLIP/FLOP for the LRCK Latch
IC12	NJM4558D	OP AMP	(1/2) OP AMP for −5 V (2/2) OP AMP for +5 V

CIRCUIT DESCRIPTION

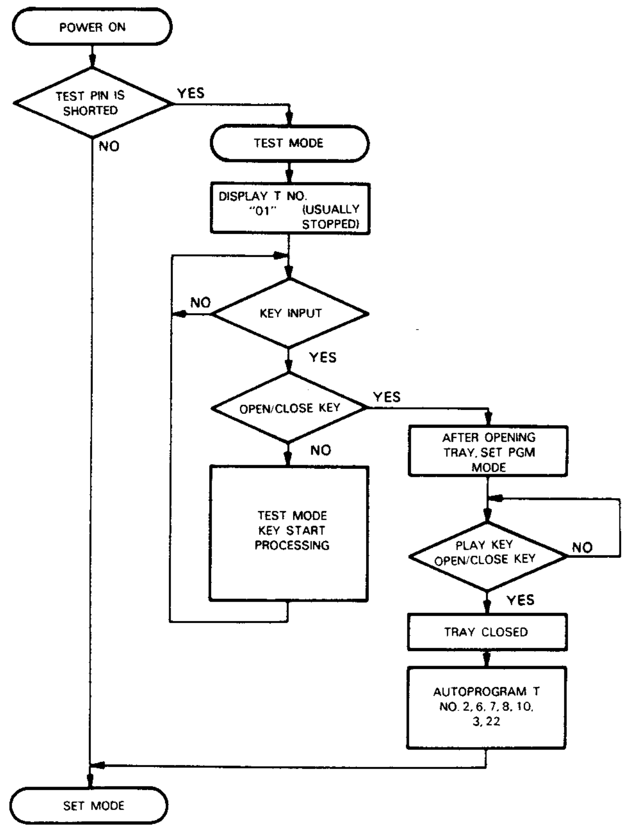
Components	Part No.	Use/Function	Operation/Condition/Interchangeability
IC13, 14	PCM56P-L-1	D/A Converter	16 bit D/A Converter
IC15, 16	NJM4565D	OP AMP	Seventh LPF AMP
IC17	μPD75212ACW-099	Microprocessor	Control of Display, Input processing of each KEY and Servo IC
IC18	M5218P	OP AMP	OP AMP for headphones
Q1	DTA124EN	Digital Transistor	Inverting Circuit to drive Q2
Q2	DTC124EN		Switch to stop control of the Data Slice Level during STOP.
Q4	2SC3940A	Transistor	Focus Coil Drive
Q5	2SB772 (Q, P)		
Q6	STA341M	Driver	Driver for Feed, Tray and Tracking Control
Q7	2SC3940A	Transistor	Disc Motor Drive
Q8	2SA1534A		
Q9	DTC124EN	Digital Transistor	For Transistor Reset
Q10	DTA124EN		ON/OFF Switch for De-emphasis
Q11	2SD1944	Ripple Filter	Ripple Filter to stablize the +5 V power
Q12	2SA954 (L, M)	Ripple Filter	Ripple Filter to stablize the −5 V power
Q13	2SA954 (L, M)	Ripple Filter	Wide use supply voltage control (−30 V)
Q14	2SK246 (Y, GR)	FET	FET for +6 V
Q15	2SA954 (L, M)	Ripple Filter	Ripple Filter to stablize the +6 V power
Q16	2SC2003 (L, M)	Ripple Filter	Ripple Filter to stablize the −6 V power
Q17	2SC945 (A) (Q, P)	Switch	Muting switch
Q18	2SC945 (A) (Q, P)	Switch	De-emphasis switch
Q19, 20	2SC2878 (B)	Switch	De-emphasis switch
Q21, 22	2SC2878 (B)	Switch	Muting switch

2. Set Mode Flow Chart
2-1. Flow Chart after POWER ON



3. Test Mode
3-1. Selection of Test Mode

Different from normal microprocessors, when in Set Mode (normal conditions) it is possible to set the IC so that it is in Test Mode all the time. This is done by shorting the Test Pin (this will only work when there is a Disc loaded).
Also, even if the Test Pin is shorted during POWER ON, the microprocessor will be in Testing Mode as usual.



CIRCUIT DESCRIPTION

3-2. Enable Keys and Functions in Test Mode

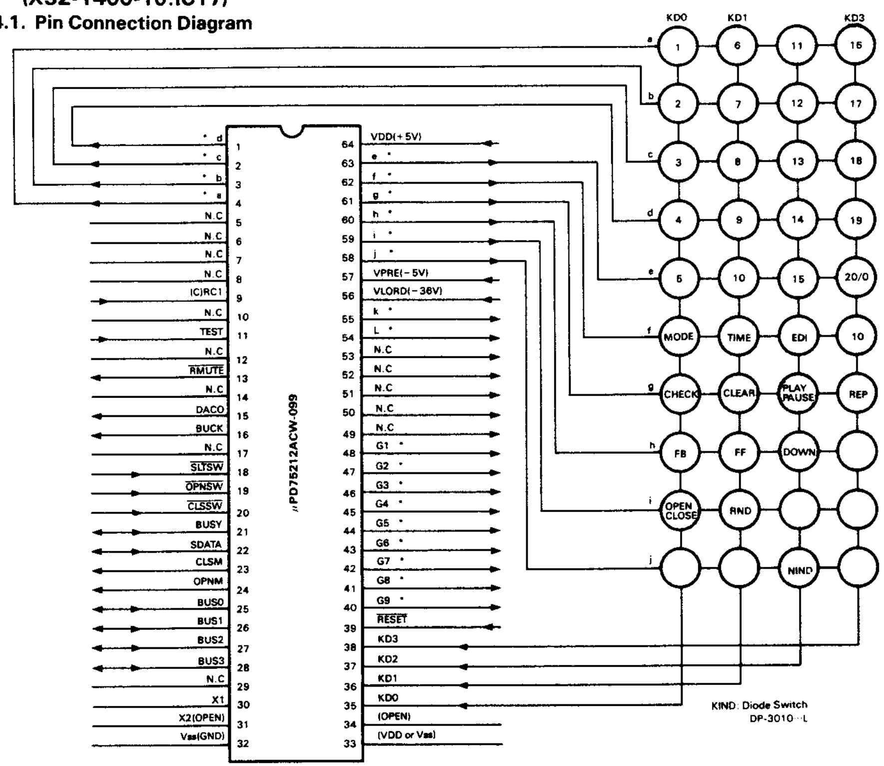
<table>
<tr><th>No.</th><th>Key name</th><th>Function</th><th>TRACK NO. display</th></tr>
<tr><td>1</td><td>PLAY</td><td>1 Focus servo .... ON
2 Tracking servo .... ON
3 Feed servo .... ON</td><td>05
Display for several seconds after completing 1, 2, 3
Display disc TRACK No.</td></tr>
<tr><td>2</td><td>CHECK</td><td>1 Focus servo .... ON
2 Tracking servo .... OFF
3 Feed servo .... OFF</td><td>03</td></tr>
<tr><td>3</td><td>CLEAR</td><td>1 Focus servo .... ON
2 Tracking servo .... ON
3 Feed servo .... OFF</td><td>04</td></tr>
<tr><td>4</td><td>STOP</td><td>1 Focus servo .... OFF
2 Tracking servo .... OFF
3 Feed servo .... OFF</td><td>01</td></tr>
<tr><td>5</td><td>REPEAT</td><td>1 Tray open
2 Laser .... ON
The REPEAT function will be cancelled when tray is pushed in and closed.
Display TRACK NO. will be " ".</td><td>02</td></tr>
<tr><td>6</td><td>▶▶</td><td>During STOP, the pick-up will move a little outward.
When feed servo ON, track gain is "H".</td><td></td></tr>
<tr><td>7</td><td>◀◀</td><td>During STOP, the pick-up will move a little inward.
When feed servo ON, track gain is "L".</td><td></td></tr>
<tr><td>8</td><td>▶▶</td><td>All FL display lit</td><td></td></tr>
<tr><td>9</td><td>◀◀</td><td>All FL display OFF</td><td></td></tr>
<tr><td>10</td><td>10 KEY (0–9)</td><td>Will jump only the following tracks
<table>
<tr><td>Key</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr>
<tr><td>Number of tracks</td><td>1</td><td>4</td><td>16</td><td>32</td><td>1000</td></tr>
<tr><td>Direction</td><td colspan="5">Outward</td></tr>
<tr><td>Key</td><td>6</td><td>7</td><td>8</td><td>9</td><td>0</td></tr>
<tr><td>Number of tracks</td><td>1</td><td>4</td><td>16</td><td>32</td><td>1000</td></tr>
<tr><td>Direction</td><td colspan="5">Inward</td></tr>
</table></td><td></td></tr>
<tr><td>11</td><td>OPEN/CLOSE</td><td>If tray is closed after open, TRACK NO. 2, 6, 7, 8, 10, 13, 22 will be programmed and the test mode will be cancelled.</td><td></td></tr>
<tr><td>12</td><td>P. MODE</td><td>TRACK NO. 2, 6, 7, 8, 10, 13, 22 will be programmed and the test mode will be cancelled.</td><td></td></tr>
</table>

Note: While in test mode, since tact key and the printed circuit board are being tested, the TRACK NO. will not be displayed.

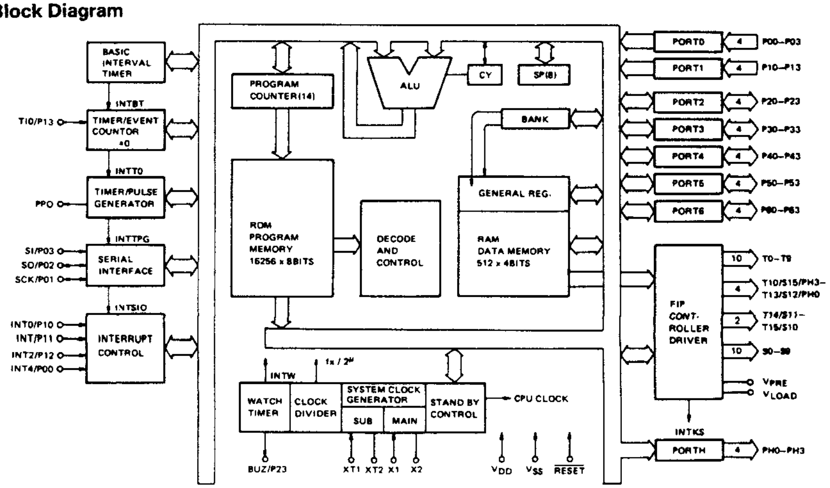
CIRCUIT DESCRIPTION

4. Microprocessor μPD75212ACW-099 (X32-1400-10:IC17)

4.1. Pin Connection Diagram



4-2. Block Diagram



CIRCUIT DESCRIPTION

4-3. Port Function Description

Pin No.	Port name	I/O	Function name	Operation
1~2	S3~S0	O	d~a	FL Segment Control Pin (used together with KEY SCAN SIGNAL)
5	P00/INT4	I	NC	No Connection
6	P01/SCK	I	NC	No Connection
7	P02/SO	I	NC	No Connection
8	P03/SI	I	NC	No Connection
9	P10/INT0	I	RCI	Remote Control Input Pin
10	P11/INT1	I	NC	No Connection
11	P12/INT2	I	TEST	Test Mode Input Pin ("H" Active)
12	P13/TIO	I	NC	No Connection
13	P20	O	RMUTE	Analog Mute Control Pin ("L" Active)
14	P21	—	NC	No Connection
15	P22	O	DACO	TC9201BF DA/CO Control Pin
16	P23	O	BUCK	TC9201BF BUCK Control Pin
17	P30	—	NC	No Connection
18	P31	I	SLTSW	Sled Limit Switch ("L" most inward)
19	P32	I	OPNSW	Tray OPEN Switch (when OPEN: "L")
20	P33	I	CLSSW	Tray CLOSE Switch (when CLOSE: "L")
21	P60	I/O	BUSY	Serial BUSY Signal Input Pin
22	P61	I/O	SDATA	Serial DATA Signal Input Pin
23	P62	O	CLSM	Tray Motor CLOSE Pin
24	P63	O	OPNM	Tray Motor OPEN Pin
25~28	P40~P43	I/O	BUS0~BUS3	TC9201BF DATA Input Pin
29	PPO	—	NC	No Connection
30	X1	I	X1	System Clock Input Terminal
31	X2	—	X2	System Clock Input Terminal
32	Vss	—	Vss	GND
33, 34	XT1, XT2	—	NC	No Connection
35~38	P50~P53	I	KD0~KD2	KEY RETURN for KEY MATRIX Input Pin
39	RESET	I	RESET	RESET Input Pin ("L" Active)
40~48	T0~T8	O	G9~G1	FL DIGIT Control Pin
49	T9	—	NC	No Connection
50~53	PH3~PH0	—	NC	No Connection
54, 55	S11, S10	O	1, k	FL Segment Control Pin
56	VLOAD	I	VLOAD	Negative Voltage for FL Drive (−29 V)
57	VPRE	I	VPRE	FL Predriver voltage
58~63	S9~S4	O	j~e	FL Segment Control Pin (used together with KEY SCAN SIGNAL)
64	VDD	—	VDD	Power (+5 V)

CIRCUIT DESCRIPTION

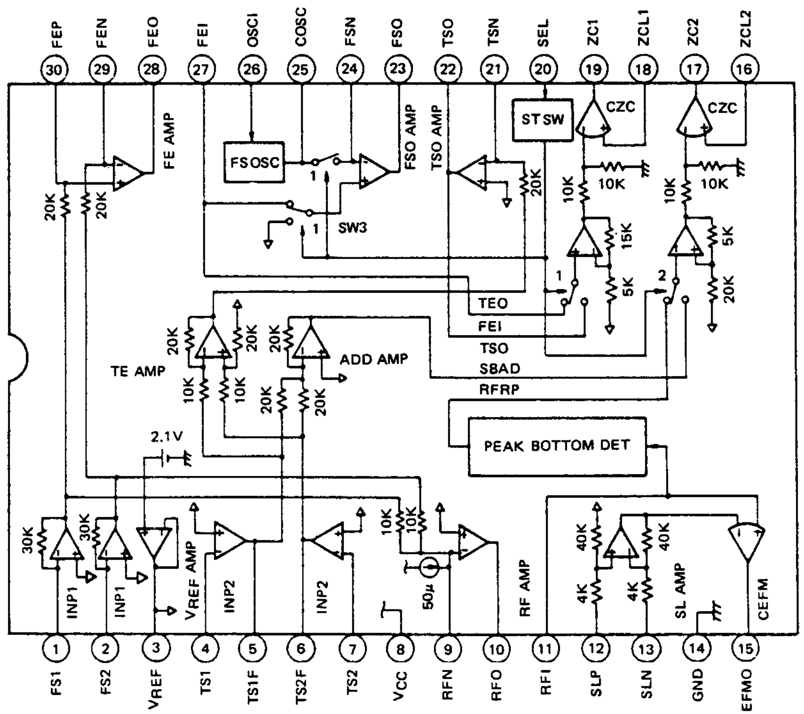
5. RF, Servo IC TA8101N (X32-1400-10:IC1)

The TA8101N IC was developed for the Focus Tracking Servo CD Player Pick-up Three-Beam Method. When used with the Servoprocessor TC9201BF, with the use of very few external components, a Servo system can be constructed to process the Servosignals.

- Being able to produce the Focus Error, Tracking Error, EFMI RF and Sub-beam Signals internally very few external components are needed.
- In the exchange of data with the Servoprocessor TC9201BF, it is to achieve smooth Focus and Tracking Servo control with the Pick-up.
- There is an internal Data Slice Circuit

Note: In the operation diagram, the C and R numbers differ from those actually used in the circuit.

5-1. Block Diagram



CIRCUIT DESCRIPTION

5-2. Pin Connections

Pin No.	Port name	I/O	Operation
1, 2	FS1, FS2	I	MAIN BEAM (I–V) CONVERTER INPUT PIN
3	VREF	O	REFERENCE VOLTAGE SUPPLY OUTPUT PIN (+2.2 V)
4	TS1	I	SUB-BEAM (I–V) CONVERTER INPUT PIN
5, 6	TS1F, TS2F	O	SUB-BEAM (I–V) CONVERTER OUTPUT PIN
7	TS2	I	SUB-BEAM (I–V) CONVERTER INPUT PIN
8	Vcc	—	POWER (+5 V)
9	RFN	I	RF AMP ANTI-PHASE INPUT PIN
10	RFO	O	RF AMP OUTPUT PIN
11	RFI	I	RF SIGNAL INPUT PIN
12	SLP	I	POSITIVE PHASE SLICE LEVEL CONTROL AMP PIN
13	SLN	I	ANTI-PHASE SLICE LEVEL CONTROL AMP PIN
14	GND	—	GND PIN
15	EFMO	O	EFM SIGNAL DATA SLICE OUPUT PIN, OPEN COLLECTOR OUTPUT
16	ZCL2	I	POSITIVE PHASE STATUS COMPARATOR INPUT PIN
17	ZC2	O	STATUS COMPARATOR OUTPUT PIN, OPEN COLLECTOR OUTPUT
18	ZCL1	I	POSITIVE PHASE STATUS COMPARATOR INPUT PIN
19	ZC1	O	STATUS COMPARATOR OUTPUT PIN, OPEN COLLECTOR OUTPUT
20	SEL	I	ANALOG SWITCH CONTROL SIGNAL INPUT PIN
21	TSN	I	ANTI-PHASE TRACKING SERVO AMP INPUT PIN
22	TSO	O	TRACKING SERVO AMP OUTPUT PIN
23	FSO	O	FOCUS SERVO AMP OUTPUT PIN
24	FSN	I	ANTI-PHASE FOCUS SERVO AMP INPUT PIN
25	COSC	O	CONDENSOR CONNECTION FOR THE PRODUCING OF THE FOCUS SEARCH SIGNAL
26	OSCI	I	INTERNAL VOLTAGE SUPPLY CONTROL PIN
27	FEI	I	FOCUS ERROR SIGNAL INPUT PIN
28	FEO	O	FOCUS ERROR AMP OUTPUT PIN
29	FEN	I	ANTI-PHASE FOCUS ERROR AMP INPUT PIN
30	FEP	I	POSITIVE PHASE FOCUS ERROR AMP INPUT PIN

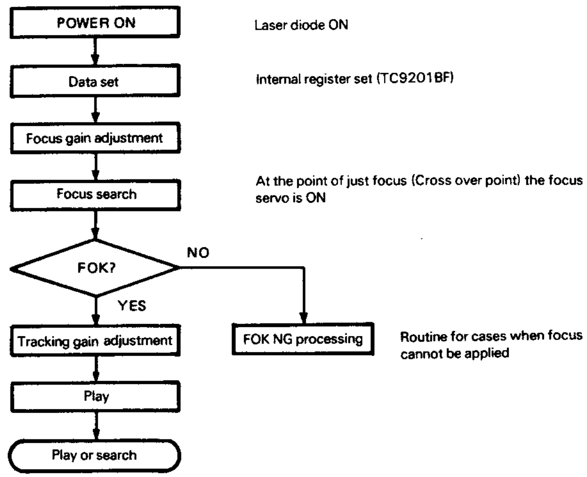
CIRCUIT DESCRIPTION

5-3. OUTLINE

The Focus Tracking Servo IC for the Pick-up AMP in the Three-Beam Method, TN8101N, is used with the Servoprocessor TC9201BF.
Also, the TA8101N consists of an RF AMP, Focus AMP, Tracking Error AMP, Focus Error Output AMP (Focus Servo), Tracking Error Output AMP (Tracking Servo), Data Slicer and Status Comparator. The following will explain the operation of these.

Diagram 5-1 shows a simple explanation of the System Mode Division in that the whole stream of the MPU processing of each operation can be seen.

CPU PROCESSING DURING POWER ON



System mode details are in reference to TC9201BF technical information

SEL Element input	System mode	Status comparator data		Details
		ZC1 side	ZC2 side	
H	Focus gain adjustment	FEI	SBAD	Correction of pick-up dispersion in the focus servo
	Focus search			Focus servo ON at cross over point
L	Tracking gain adjustment	TSO	RFRP	Correction of pick-up dispersion in the tracking servo
HiZ	Nonplay, normal play		SBAD	Play (detection of scratches and shocks)
L	Special play		RFRP	Refer to TC9201BF technical information
L	Tracking search			Song beginning, fast forward, rewind

FEI: focus error signal, SBAD: sub-beam summing signal
TSO: tracking error signal, RFRP: RF ripple signal

Diagram 5-1 System Mode Division

5-4. Operation Information

• **RF AMP**

The 1/4 pin photodiode output for the Main Beam Detection of the Pick-up Three-Beam Optical Method is shown in Diagram 5-1. Pins FS1 and FS2 of TA8101N are directly connected to the above output so that (B+D) and (A+C) signals are input here. The (B+D) and (A+C) signals are converted from current to voltage in Converter 1a and 1b (I−V). The summed signal (A+B+C+D) passes through the RF AMP and is output from the RFO pin. Since the pin photodiode is an equalized constant voltage supply, the curcuit is designed so that the insertion loss of the gain to the RFO output will be typically 81 kΩ (R2, C1 excluded) when the external feedback resister (VR1+R1) of the RF AMP is 27 kΩ.

The insertion loss for FS1 or FS2 to RFO is calculated as follows:

$$R_T(RF) = 3R_{NF1} = 3 \times 27\,k\Omega = 81\,k\Omega$$

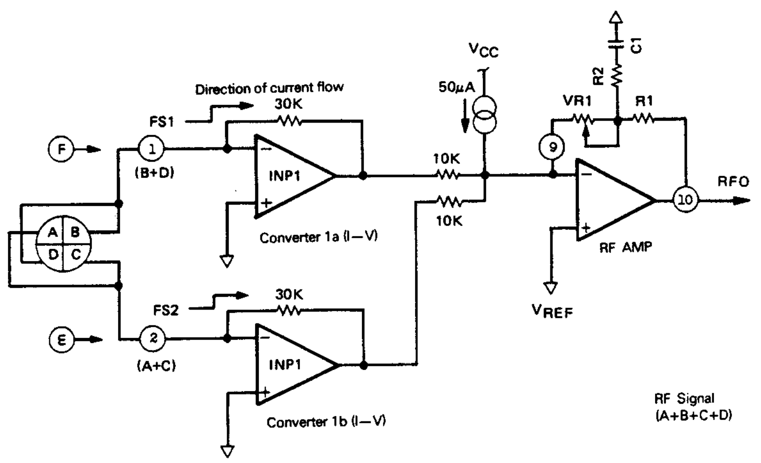


Diagram 5-1 RF AMP Construction

• **Focus Error AMP**

The signal difference {(A+C) − (B+D)} between Converter 1a (I−V) and Converter 1b (I−V) is output from the FEO pin after passing through the Focus Error AMP.

The circuit is designed so that the gain from the Converter (I−V) to FEO will have a typical insertion loss of 123 kΩ (external resistance is RNF2 = VR2 = VR3 = VR4 = 82 kΩ).

The output from the FEI attenuator is adjusted for focus gain in TC9201BF. From the two analog switches, FEL1 and FEL2, it is attenuated to about 0.8 Vp-p, the Pick-up dispersion is corrected and then it is input to the Focus Servo AMP.

VR2 is used as the balancer for the Focus Error Signal where the offset is adjusted.

The insertion loss for FS1 or FS2 to FEO is calculated as follows:

$$R_T(FE) = 1.5\,R_{NF2} = 1.5 \times 82\,k\Omega = 123\,k\Omega$$

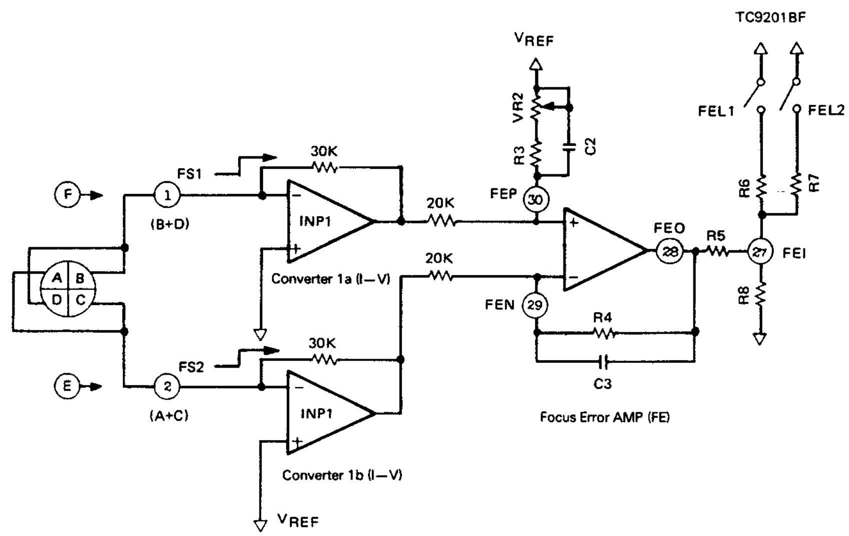


Diagram 5-2 Focus Error AMP Construction

CIRCUIT DESCRIPTION

Setting of R5 ~ R8 for Focus Gain Adjustment
The following simply explains the operations for Focus Gain Adjustment and the method for setting R5 ~ R8.

1) Focus Gain Adjustment

- As soon as Focus Gain Adjustment is started, FEL1 and FEL2 of TC9201BF become VREF.
- During Focus Gain Adjustment the internal Focus Error Signal of TC9201BF is in Peak Data Hold Mode. The Peak Data achieved is set to the internal resister.
- As soon as Focus Gain Adjustment is complete, the Peak Data achieved in TC9201BF is decoded. FEL1 and FEL2 are then set to either one of the conditions shown in Diagram 5-4. (Refer to TC9201BF Technical Information for details)

2) Setting Method of R5 ~ R8

- The peak values of the Focus Error Signal within the Pick-up dispersion during VREF, the compared range of R5 ~ R8 of pins FEL1 and FEL2 are set as shown in Diagram 5-4 (R6 is self setting).
- Each Focus Error Signal within the range is set with R6 ~ R8 to about 0.4 Vp-o (about 0.8 Vp-p) peak value at the FEI pin (Only R6 > R7). The attenuate amount of the Attenuator in Diagram 5-3 is as follows.

$$K_F = \frac{V_{EF1}}{V_{EFO}} = \frac{1}{1 + \frac{R5}{R6} + \frac{R5}{R7} + \frac{R5}{R8}}$$

Note: The peak value of the Focus Error Signal of the FEO pin is set so that the previous stage gain is more than 0.4 Vp-o within the Pick-up dispersion range.

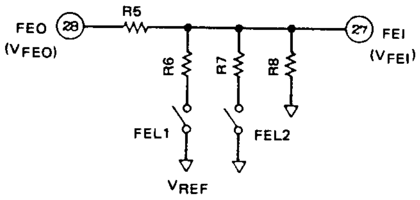


Diagram 5-3 Focus Gain Adjustment Construction

FEL1	FEL2	FEI Peak Value (Vp-o) (X VREF)
		0.25
VREF	VREF	0.156
Hi Z	VREF	0.125
VREF	Hi Z	0.0937
Hi Z	Hi Z	0

Diagram 5-4 Pin FEL1 and FEL2 Conditions

CIRCUIT DESCRIPTION

- **Tracking Error AMP**

As shown in Diagram 5-5, the Pin Photodiode output for the detected Pick-up Sub-beam of the Three-Beam Optical Method are connected directly to the TS1 and TS2 pins where the F and E signals are input.

After being converted from Current to Voltage in Converter 2a and 2b (I—V), the difference of F and E signals (F—E) is passed through the TE AMP to be supplied to the inner circuit. The VR3 of Converter 2b (I—V) is used as the Tracking Error Signal balancer.

The insertion loss from TS1 or TS2 to TEO is calculated as follows:

$$R_T(TE) = 2R_{NF3} \ (R_{NF3} = R9 = VR3 + R10)$$

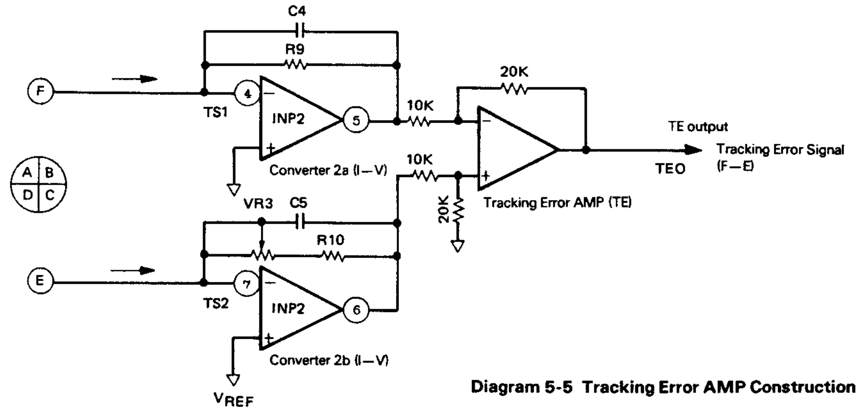


Diagram 5-5 Tracking Error AMP Construction

- **Focus Error Output AMP**

Diagram 5-6 is constructed of the Triangle Tooth Wave Producing Circuit, the FSO AMP used as the phase compensator for Focus signals and the control circuit that switches the Focus Servo Signal and the Focus Search Signal. The modes of the switch positions are as shown in Diagram 5-2 where the FSO AMP is used as an Inverting AMP during Focus Search and as an Non-inverting AMP during Normal Play.

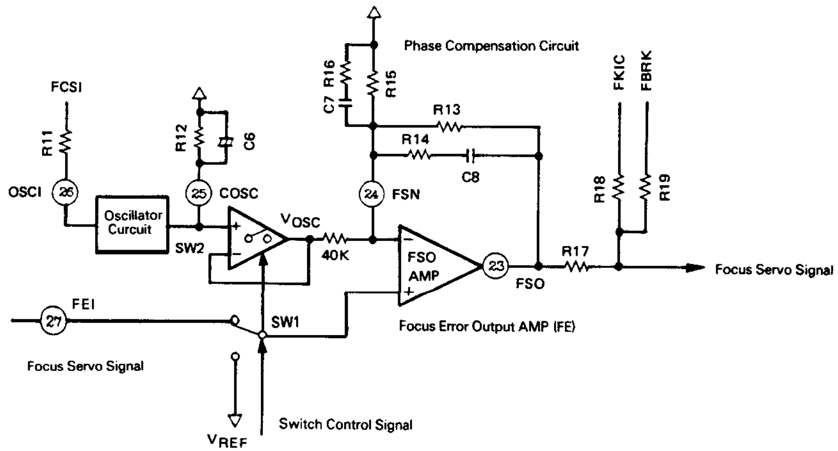


Diagram 5-6 Focus Error Output AMP Construction

CIRCUIT DESCRIPTION

Diagram 5-7 shows the timing of each part.

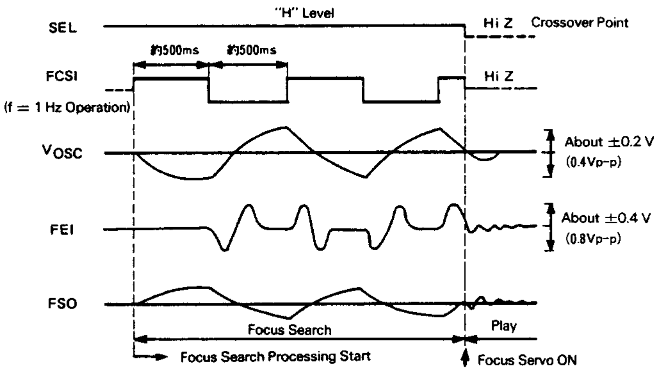


Diagram 5-7 Each Timing of the Focus Servo Signals

SEL	SW1	SW2	System Mode
H	VREF	ON	Socus Search
HiZ	FEI	OFF	Normal Play
L	FEI	OFF	Search

Diagram 5-2 Switch Position

A simple explaination of each part is as follows.

1) Triangle Wave Emitting Circuit
The Triangle Wave is emitted in the Oscillator Circuit (COSC) into charge and discharge which is then adjusted in RCSI.
From this the reference is set by COSC and RCSI during Focus Search.
ROSC is to keep the reference point stable during Focus Search Start where it is the discharge resistor for COSC.
Each current VOSC can be calculated as follows:

$$I_{CSI} = \frac{V_{CC}}{2 \cdot R_{CSI} + 10 \times 10^3}, \quad I_{OSC} = \frac{1}{4} \cdot I_{CSI}.$$

$$V_{OSC} = I_{OSC} \cdot \frac{R_{OSC}}{1 + j\omega C_{OSC} \cdot R_{OSC}}$$

Furthermore, during Focus Search, the VOSC Focus Lense should be set at a level where there is ample space to move vertically.

2) FSO AMP
Set the Focus Actuator Gain Characteristics, the Gain together with the Phase Characteristics and the Gain Compensation Reference.

3) Control Circuit
This circuit switches the input to the Focus Error Output AMP between Focus Servo and Focus Search signals. The Switch Position is set as in Diagram 5-2.
The Switch Position is set with SEL and can correspond to three system modes.
The Focus Search Processing Mode is done after Focus Gain Adjustment as shown in Diagram 5-1 (Page 18). FKIC signal is used during Focus Gain Adjustmeent and FCSI and FBRK signals are used during Focus Search.
Normally, FKIC, FCSI and FBRK signals are HiZ.

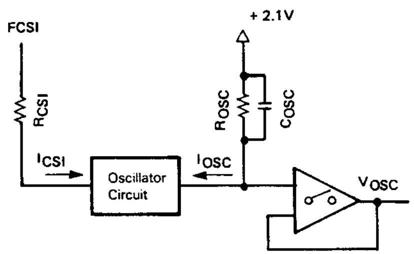


Diagram 5-8 TriangleWave Producing Circuit

CIRCUIT DESCRIPTION

• Tracking Error Output AMP

By inputing the Tracking Error Signal just explained, the Tracking Servo Signal is emitted in reference with VREF. It is designed so that the gain upto the TSO including the TE AMP will have any insertion loss of 540 kΩ (Feedback Resistance: RNF3 = R9 = R10 + VR3 = 270 kΩ, RNF4 = R20 + R21 = 20 Kohm). (Note: RNF4 does not included R22 and R23)
The level of the TSO amount is set by using the analog switches TEL1 and TEL2 of TC9201BF to do Tracking Gain Adjustment. The TSO output voltage is about 8 Vp-p at this time.

Futhermore, the Pick-up Tracking Actuator Gain Characteristics and the Phase Characteristics are to be used together for each reference of the Phase Compensation Circuit.
For detailed information of the operation of TESH, TEOF, TGUL, TGUH and DFCT pins, refer to the TC9201BF technical information.
The insertion loss from TS1 or TS2 to TSO can be calculated as follows:

$$R_T(TS) = \frac{R_{NF3} \times R_{NF4}}{10 \times 10^3}$$

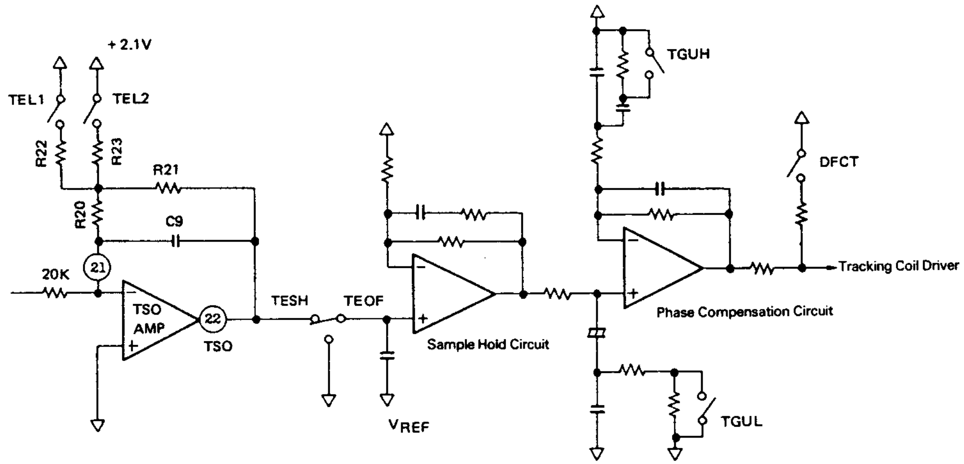


Diagram 5-9 Tracking Error Output AMP Construction

CIRCUIT DESCRIPTION

Setting of R20 ~ R23 for Tracking Gain Adjustment

The following simply explains the operations for Tracking Gain Adjustment and the method for setting R20 ~ R23.

1) Tracking Gain Adjustment Operations

- As soon as Tracking Gain Adjustment Operations are started, TEL1 and TEL2 of TC9201BF become HiZ.
- During Tracking Gain Adjustment the internal Tracking Error Signal of TC9201BF is in Peak Data Hold Mode. The Peak Data achieved is set to the internal resister.
- As soon as Tracking Gain Adjustment is complete, the Peak Data achieved in TC9201BF is decoded. TEL1 and TEL2 are then set to either one of the conditions shown in Diagram 5-11. (Refer to TC9201BF Technical Information for details)

2) Setting Method of R20-R23

- The peak values of the Tracking Error Signal within the Pick-up dispersion during HiZ, are set to within the range of R20 ~ R23 of pins TEL1 and TEL2 as shown in Diagram 5-11.
- Each Tracking Error Signal within the range is set with R22 and R23 to about 0.4 Vp-o (about 0.8 Vp-p) peak value at the TSO pin.
  The attentation amount of the Attenuator in Diagram 5-10 is as follows:

$$K_T = \frac{V_{TSO}}{V_{TEO}} = -\left\{\frac{R20+R21}{20\times10^3} + \frac{R20\cdot R21}{20\times10^3}\left(\frac{1}{R22}+\frac{1}{R23}\right)\right\}$$

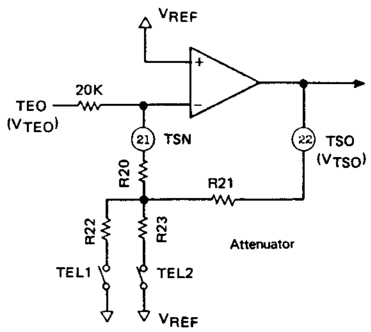


Diagram 5-10 Tracking Gain Adjustment Construction

TEL1	TEL2	TSO Peak Value (Vp-p) (X VREF)
Hi Z	Hi Z	0.25
VREF	Hi Z	0.141
Hi Z	VREF	0.109
VREF	VREF	0.078
		0

Diagram 5-11 TEL1 and TEL2 Pin Conditions

CIRCUIT DESCRIPTION

- **Data Slicer**

The Data Slicer changes the EFMI RF Signal into a Digital Signal.

By using the fact that averagely EFMO is equal to Zero DC during H and L periods, the ELMO with the AC content excluded for the Slice Level of the Data Slicer is fedback and used.(Diagram 5-13). When using this for the Digital PLL Circuit of TC9201BF, the Slice Level is fixed.

This is possible because TC9201BF has an internal Data Correction Curcuit and thus removes problems coming from Disc Production dispersion of a symmetry jitter (No adjustment).

Also, the EFMO is used for Open Collector Output. It is suggested to connect a Pull-up Resister of roughly 2.2 kΩ to the Digital Supply Voltage to assist the EFMO Start Up Characteristics.

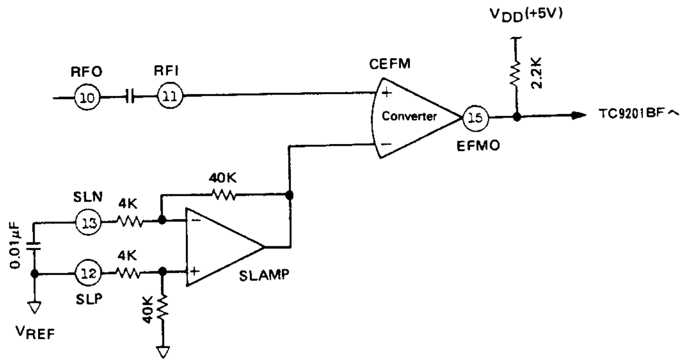


Diagram 5-12 Data Slicer Construction

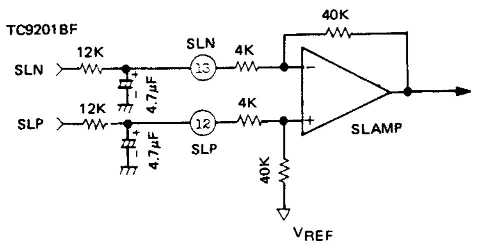


Diagram 5-13 Slice Level Construction

CIRCUIT DESCRIPTION

● **Status Comparator**

The AD converted data of the FEI, TSO, SBAD and RFRP signals for each mode (in Diagram 5-1, Page 18) is needed internally for TC9201BF. The Status Converter is used for this AD conversion. With the Up/Down Counter and DA Converter in TC9201BF and the Status Converter in TA8101N working together a "Follow-up/Comparator" AD Converter is constructed. Thus the four signals are digitalized (5 bit data) as shown in Diagram 5-14 (Refer to TC9201BF Technical Information for further details).

Also shown in Diagram 5-14, the circuit is designed so that the Dynamic Range of the Comparator Input is 0 — VREF (+2.2 V).
Since the Comparator (CZC) Output is an Open Collector Output, a 10 kΩ Pull-up AMP should be used.

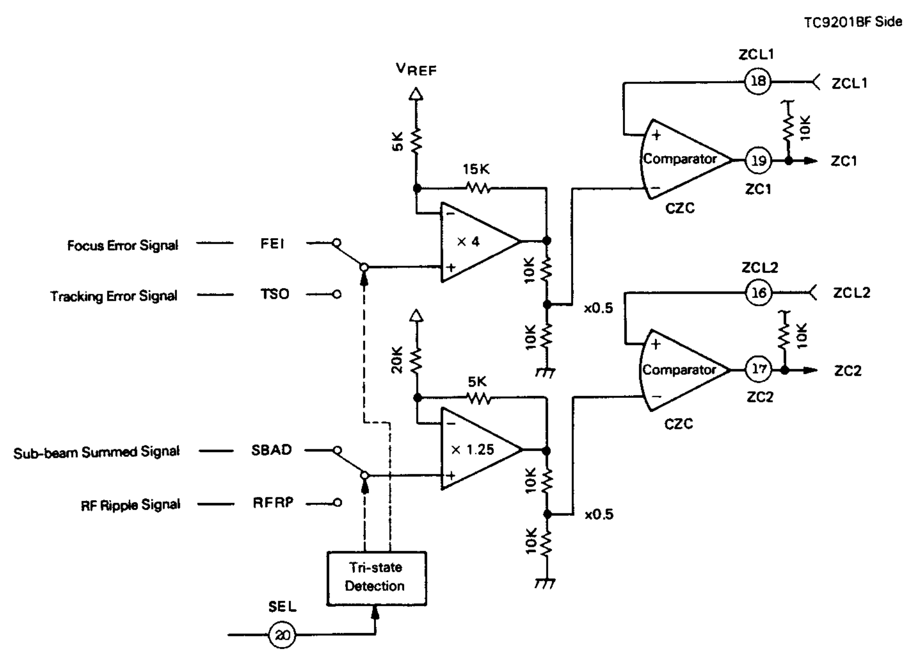


Diagram 5-14 Status Comparator Construction

CIRCUIT DESCRIPTION

1) Sub-beam Summed (SBAD) Signal Emitting Circuit
The Sub-beam Summed (SBAD) Signal is a Summed Signal of Converter 2a and 2b (I—V) where the Focus ON/OFF Half Normal Signal and the Disc Scratches (drop out) detection information is used.

The SBAD signal, as shown in Diagram 5-1 (page 18), is selected from the System Mode when needed, passed through the Status Comparator (CZC) and is supplied to the CMOS Servo Processor, TC9201BF.

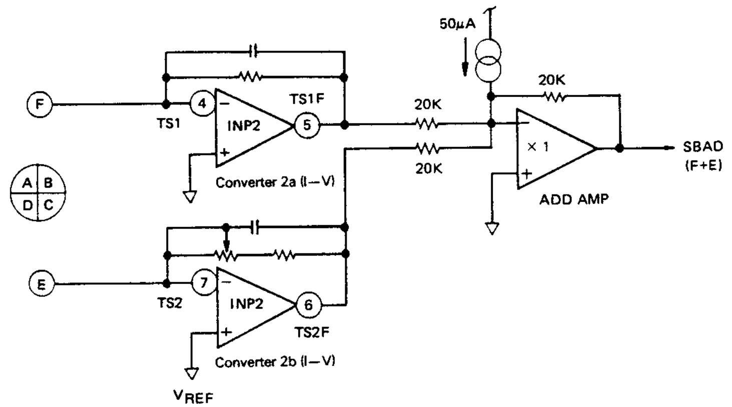
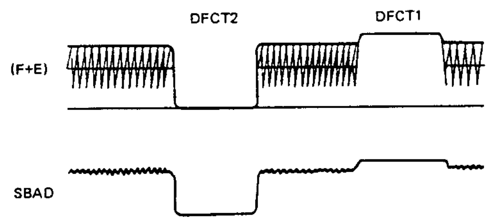


Diagram 5-15 SBAD Signal Emitting Curcuit Construction



(DFCT1 . . . . Black Dot at Read Out Side.)
(DFCT2 . . . . . . Interruption in Information Layer.)

Diagram 5-16 SBAD Signal Operation Wave Forms

CIRCUIT DESCRIPTION

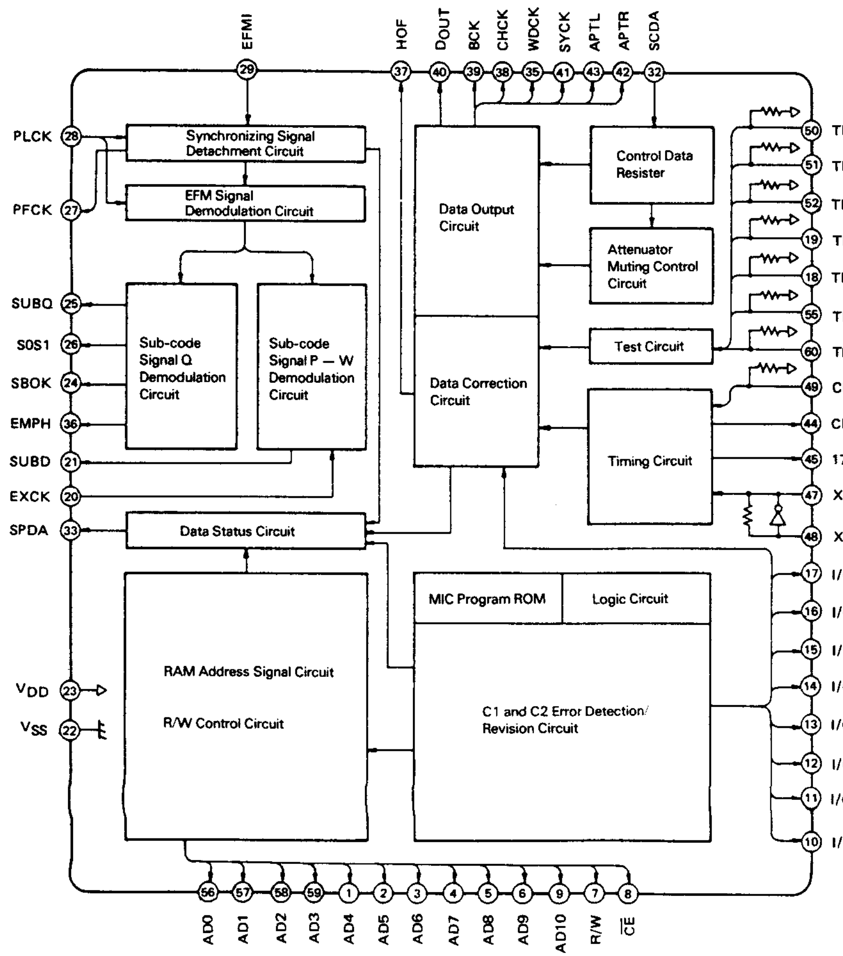
6. Digital Signal Processing LSI TC9200BF (X32-1400-10:IC4)

The TC9200BF is an LSI developed for Synchronizing Detachment, EFM signal demodulation, Error Detection and Revision.

A simple CD Player Processor can be constructed by using the TC9200BF.

- Synchronizing Pattern Detection, Synchronizing Signal Protection and interpolar operation are made possible.
- Equipped with an internal Sub-Code Signal Demodulation Circuit. Interface with the CPU is easily made.
- By using the CIRC Revision Logic, revision capacity of four C1 and two C2 revision sections (complete revision of up to eight frame BUST Error) are available.
- Equipped with ±5 Frame Jitter Correction Capacity
- Equipped with an internal Muting Signal Detection Circuit (Smooth Muting Operation with the use of Zero Cross Detection of the output data)
- −12 dB attenuation is possible.

6-1 Block Diagram



DP-1510

CIRCUIT DESCRIPTION

2) RF Ripple (RFRP) Signal Emitting Curcuit:
RF Detection Peak/Bottom Detection

The RF Ripple (RFRP) Signal is On-Track Information that is passed through the Status Converter (CZC) before being supplied to the CMOS Servo Processor, TC9201BF. When needed, the RFRP Signal is selected from the System Mode, as shown in Diagram 5-1 (page 18). During Tracking Gain Adjustment, the Focus ON/OFF Half Normal Information and during Tracking Search, the Tracking Error Signal are used for Track Count Information and Search Converged Information.

The RF Ripple Signal is achieved by taking the differential of the RF Signal Peak and Bottom Hold Signals.

In the actual RF Signal there is Low Frequency Fluctuation but by taking differential, the fluctuation is taken out and thus a stabilized RFRP wave form is achieved.

(PEAK BOTTOM DET)

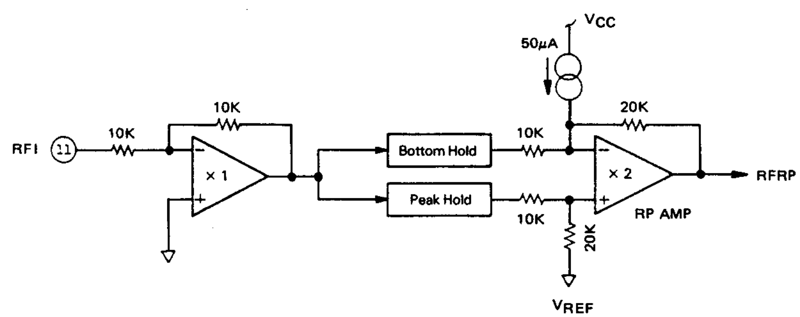


Diagram 5-17 RFRP Signal Producing Circuit Construction

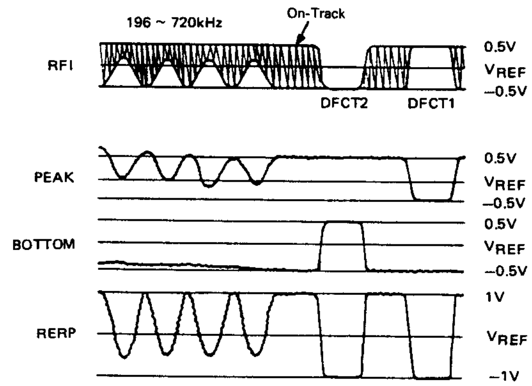


Diagram 5-18 RFRP Signal Operation Wave Form

6-2. Pin Configuration

NOTE: EXTERNAL RAM = 8 BIT × 2K

Pin No.	Port name	I/O	Operation
1 ~ 6	AD4 ~ AD9	O	External RAM Address Signal Output Pin
7	RW	O	External RAM Read/Write Signal Output Pin
8	CE	O	External RAM Chip Enable Signal Output Pin
9	AD10	O	External RAM Address Signal Output Pin
10 ~ 17	I/O-7 ~ I/O-0	I/O	External RAM Data Bus Line
18, 19	TES5, TES4	I	Test Pin. Normally used in "H" or OPEN
20	EXCK	I	Sub-code P–W and S0+S1 Data Reading Clock Input Pin
21	SUBD	I	Sub-code P–W Output Pin. Data set with the internal resister at PFCK fall point
22	Vss	—	GND Pin
23	VDD	—	Power (+5 V)
24	SBOK	O	Sub-code Signal Q Data CRC Check Decision/Result Pin (Normal "H", Error "L") The Decision/Result is output one block prior to the 80-bit Q Data being output.
25	SUBQ	O	Sub-code Signal Q Output Pin. PFCK fall edge synchronized before Q Data is output.
26	S0, S1	O	Sub-code Sink S0 and S1 Pin. When Sub-code Sink is detected in S0 or S1, "H" level is output for that frame (PFCK fall is edge synchronized)
27	PFCK	I	Play Mode Frame Cycle Signal Output Pin. f = 7.35 kHz (Duty Cycle = about 50%)
28	PLCK	I	Data Reading Clock Input Pin. Clock produced the PLL Circuit in reference to the RF signal played from the DISC During PLL Phase Clock: 4.32 MHz (Duty Cycle = 50%)
29	EFMI	I	EFM Signal Input Pin. Synchronized to the PLCK and then input.
30, 31	NC	—	No Connection
32	SCDA	I	Control Data Serial Input Pin. Serial Data Input of Each Frame from TC9201BF
33	SPDA	O	Processor Status Output Pin. Information such as Synchronized conditions in Frame Units, Revised Decision/Result Processing, Memory Buffer Capacity are serial output.
34	COFS	O	Revision Mode Frame Synchronized Output Pin. f = 7.35 kHz ((X'tal divided)
35	WDCK	O	Word Clock Output Pin. Clock divided 16 times from BCK. (Duty Cycle = 50%) f = 88.2 kHz
36	EMPH	O	Specified Emphasis ON/OFF Signal Output Pin. Confirmation of existence of Emphasis for the Q Data Control Bit (When "H", Emphasis ON) When the CRC Decision/Result is confirmed as OK twice, Emphasis is confirmed.
37	HOF	O	Output Data Correction Flag Output Pin. Flag added every 8 bits, at the same time as data output. LSB and MSB side are synchronized with the SYCK fall in Flag order.
38	CHCK	O	Channel Clock Output Pin. This is the WDCK clock signal divided twice, when "L" level LCH and when "H" level RCH data is output. f = 44.1 kHz (Duty cycle = 50%)
39	BCK	O	Bit Clock Output Pin. f = 1.4112 kHz (Duty Cycle = 50%)
40	DOUT	O	Data Output Pin. The BCK fall is edge synchronized from the MSB side to be serial output.
41	SYCK	O	Symbol Clock Output Pin. This is the clock divided eight times from BCK. f = 176.4 kHz (Duty cycle = 50%)
42	ARTR	O	RCH Data Aperture Signal Output
43	APTL	O	LCH Data Aperture Signal Output
44	CK8M	O	8M Clock Output Pin. (X'tal 16.9344 MHz clock divided twice)
45	17MO	O	17M Clock Output Pin. (X'tal 16.9344 MHz Buffer Output)
46	NC	—	No connection
47	X-O	O	Crystal Resonator Connection Pin. The Crystal Resonator provides the System with the desired Clock Frequency (X'tal 16.9344 MHz)
48	X-I	I	Crystal Resonator Connection Pin. The Crystal Resonator provides the System with the desired Clock Frequency (X'tal 16.9344 MHz)
49	CKSE	I	Clock Selection Pin. When the X-I Input Clock is "H" or OPEN then 16.9344 MHz, when "L" then 8.4672 MHz is selected.
50 ~ 52	TES1 ~ TES3	I	Test Pin. Normally used in "H" or OPEN.
53	VDD	—	Power (+5 V)
54	Vss	—	GND Pin.
55	TES6	I	Test Pin. Normally used in "H" or OPEN
56 ~ 59	AD0 ~ AD3	O	External RAM Address Signal Output Pin
60	TES7	I	Test Pin. Normally used in "H" or OPEN

6-3. Operation Information

6-3-1. EFM Signal Demodulation Mode Block Operation

- **Synchronizing Signal Detachment Circuit**

The Synchronizing Signal Detachment Circuit is divided into the Synchronizing Pattern Detection and Sychronizing Signal Protection Interpolar Circuits. The operation of each of these is shown as follows.

1) Synchronizing Pattern Detection Circuit

The detection of whether there are two consecutive patterns of 11T (1T = 1PLCK) from edge to edge in the HF Signal Picked-Up from the Disc is done thus creating the Frame Synchronizing Signal.

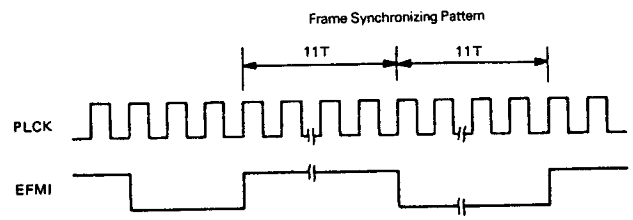


Diagram 6-1 Input Signal Timing Chart

2) Synchronizing Signal Correction/Interpolarity Circuit

The Frame Synchronizing Signal shown in Diagram 6-1 is used in the internal Demodulation Circuit for synchronizing but there is a possibility of miss detection due the to quality of the input signal if the Synchronized Signal is used as it is.

Therefore the following powerful Synchronizing Signal Correction Circuit is needed.

The Synchronizing Signal Detachment Circuit is shown in Diagram 6-2.

As shown in this Diagram, the whole circuit is constructed of a 1/588 Division Curcuit, a Gate Signal Producing Circuit (WIND Gen.) and an Off Synchronizing Counter (NSFC).

Normally the Gate Signal (R-WIND) produced from the IFC output used for correction of the Proper Frame Synchronizing Signal (Only the Synchronizing Signal input to R-WIND is used for synchronizing the Demodulation Circuit).

When a non-synchronized condition continues, such as during POWER ON, when a Bust Error occurs or when the PLL circuit is instable, P-WIND from the WIND Gen. Output and Off Synchronizing Frame Counter (NSFC) are put into operation to effortlessly synchronize the condition.

See the following simple explanation for the steps taken in synchronizing.

1 The setting of the number of times of Off Synchronized Detection, N, is done by selecting one of the 2-bit N = 2, 4, 8, 12 in ESGL and ESGM.

2 When a condition where the Frame Synchronizing Signal does not enter R-WIND continues and NSFC output become N, the NSFC operation stops. At the same time the FSPS Ouput Level changes from "L" to "H" turning on each Correction Circuit.

3 When the FSPS Level changes to "H", P-WIND starts the SET RESET and the Frame Synchronizing Signal is synchronized with IFC.

4 When the Frame Synchronizing Signal is input to R-WIND, it is judged as the Proper Synchronizing Signal and the synchronized NSFS of IFC is cleared.

At this time, the FSPS Level changes to "L" and the Input Synchronized Pattern from the internal system completes synchronizing.

Also, besides the FSPS there is the FSLO Status Flag where FSLO and FSPS are output through the SCDA pin.

ESGM and ESGL are input to the SCDA pin from TS9201BF.

WSEG details are available on Page 40.

ESGM	ESGL	N
1	1	2
1	0	4
0	1	8
0	0	12

WSEG	R-WIND Width
1	±7 PLCK
0	±3 PLCK

It is possible to change the R-WIND Width with WSEG.

Diagram 6-1

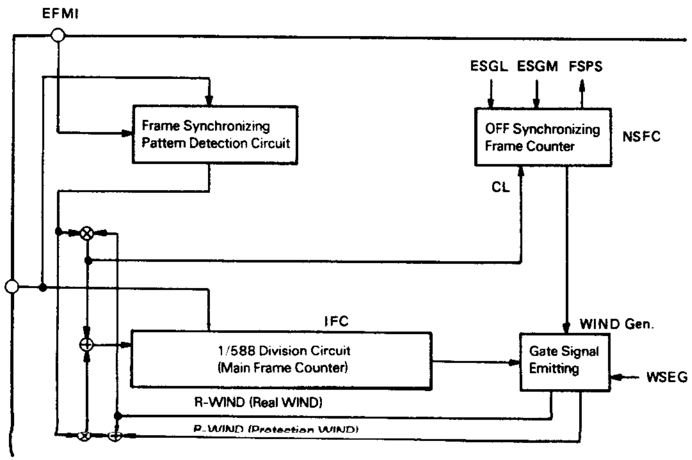


Diagram 6-2 Synchronizing Signal Detachment Circuit Construction

• EFM Signal Demodulation Circuit

The EFM Signal Demodulation Circuit, with reference to the Main Frame Counter (IFC) of the Synchronizing Detachment Circuit, consecutively demodulates the Sub-Code Signal within each frame and the 32 Symbol Data (Restored to digital signal from EFMI) from 14 bits to 8 bits.

The demodulated data is set to the internal latch, and written into the external RAM by using Address A0 — A10 from the RAM Address Control Circuit, the Write Signal (RW = L), and Chip Enable Signal (CE = L) in one symbol (8 bit) units through IO 0 — 7.

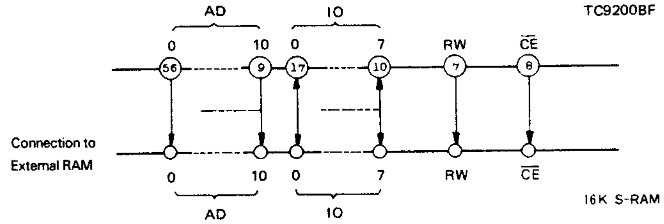


Diagram 6-3

• Sub-Code Signal Demodulation Circuit

The 8-bit data in each frame for control and diplay in sub-code P, Q, R, S, T, U, V, W, is set to the internal resister before the leading edge of PFCK (pin 27). This is synchronized with the trailing edge of the read clock input from the EXCK pin. This is emitted in serial from the SUBD pin. Each condition for the output data is as follows.

SUBD OUTPUT	S0, S1 OUTPUT TIMING	NORMAL TIMING
P	When S0 output, "H"	Sub-code P Data
Q	When S1 output, "L"	Sub-code Q Data
R ~ W	Not Fixed	Sub-code R ~ W Data

Diagram 6-2 SUBD output data details

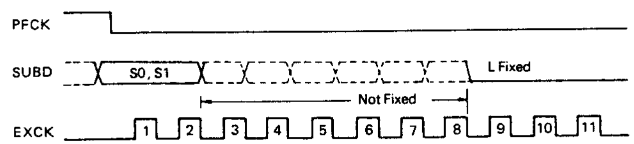


Diagram 6-4 Timing Example (1): During S1 Detection (Only Detect S0 one frame before)

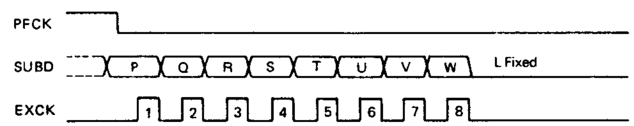


Diagram 6.5 Timing Example (2): Normally

• Sub-code Signal Q Data Demodulation Circuit

The Sub-code Signal Q Data Demodulation Circuit demodulates the Q Data of the Sub-code Signal in units of 98 frames. It then does Error Detection/Judgement Processing of each data before output.
In each system, the Sub-code Synchronizing Signal is synchronized at S0 and S1, so that the Error Detection/-Judgement Processing can be done by consecutively reading CRCC 80-bit Q Data. From the SBOK pin Error Detection/Judgement results and from the SUBQ pin the demodulated Q Data are synchronized with the PFCK leading edge and then output.

- S0, S1: The level of the Sub-code Synchronizing Signal Output is "H" in the frame during S0 and S1 detection.
- SBOK: The Sub-code Q Data CRCC Check Judgement Result Output is "H" level during No Error.

Each signal from S0 S1, SUBQ, SBOK and PFCK are moved to TC9201BF.
The 80-bit Q Data is initially read into the internal RAM of TA9201BF.
When needed, this data is sent from the bus line to the MPU through the CPU Interface.

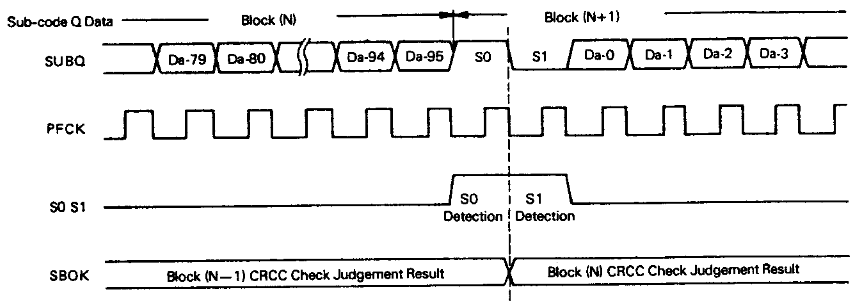


Diagram 6-9 Sub-code Q Data Output Timing

• Other

In the Control Bit Information of the Sub-code Signal Q Data, the Emphasis ON/OFF Judgement Output is output through the EMPH pin.
When the level of the EMPH Output is "H", the Emphasis is ON.

When two blocks (two 98 frames) of Q Data CRCC Check Judgement Results (SBOK output) are found to be consecutively normal, the data is valid.

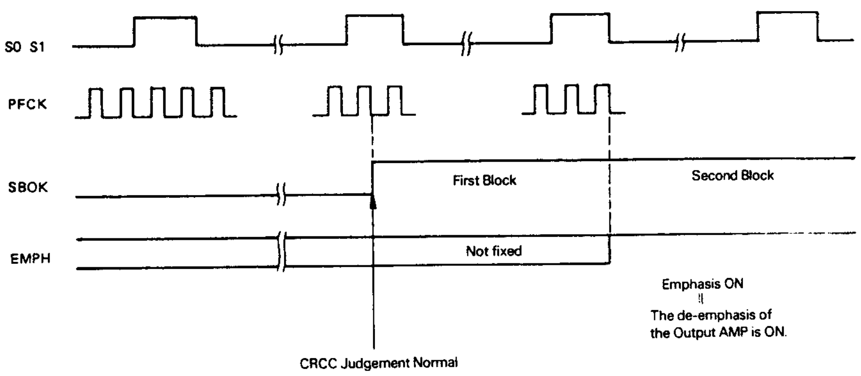


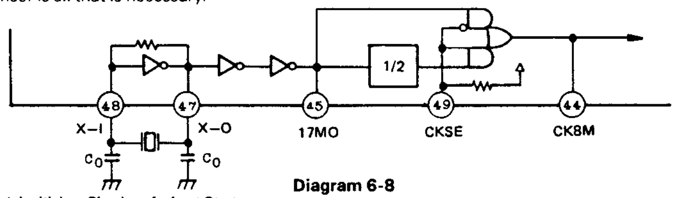
Diagram 6-7 Emphasis ON/OFF Output Timing

6-3-2 Error Detection, Delete and Correction Processing Mode Block Operation Information

• Timing Circuit

The Clock Signal needed for internal operation is as shown in Diagram 6-8, where that by only connecting a crystal and condensor is all that is necessary.

The selection of the frequency of the crystal is done by setting the CKSE pin.
CKSE = "L" fx'tal = 8.4672 MHz
CKSE = "H" fx'tal = 16.9344 MHz



Note: Use a crystal with low CI values for best Start-up Characteristics

Diagram 6-8

• RAM Address Control Circuit

TC9200BF reads modulated input data by use of the external RAM (8-bit × 2 k) address control and does deinterleave processing.
Input Data Jitter Absorbing Capability for the memory has a capacity of ±5 frames; constant surveillance (Differential Detection) of the Input and Output Data Rates are provided in the design for best results of the RAM Address Control.
In response to the condition of buffer capacity, the following DIV+ and DIV− signals are output. DIV+ and DIV− are used for Disc Motor CLV Servo Control and including the motor a Field Back Loop is constructed.
Therefore, the actual Input Data Jitter Absorbing Capability is being enhanced.
Also, when the buffer capacity exceeds ±5 frames, it is taken as Buffer Over thus the BUF-OV Signal is output. During BUF-OV, DIV+ and DIV− are reset, the Mute On Buffer capacity is forced to become −1. BUF-OV is thus cancelled, and the RAM Address Control is continued.

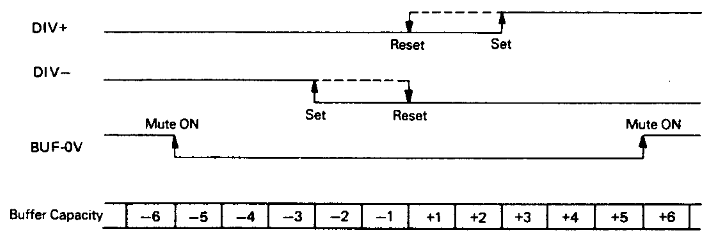


Diagram 6-9 Control Signal DIV+, DIV−, BUF-OV Output Timing

It is possible to externally monitor the Buffer Capacity by checking the Data Status Signal Output from the SPDA pin. As shown in Diagram 6-3, three bits, BUF 2 − 0, are output.

BUF2	BUF1	BUF0	Buffer Capacity	BUF2	BUF1	BUF0	Buffer Capacity
1	1	1	−1	0	0	0	+1
1	1	0	−2	0	0	1	+2
1	0	1	−3	0	1	0	+3
1	0	0	−4	0	1	1	+4
0	1	1	−5	1	0	0	+5

Diagram 6-3 Buffer Capacity Output Data

CIRCUIT DESCRIPTION

• C1 and C2 Revision Circuit

Error Detection and Revision Processing in the CD is done in two places, C1 and C2.

1) C1 Detection/Revision Section

For C1 Revision Processing, the Error Detection in each frame of the input data for High Priority Items is done as follows: one High Priority Item is deleted and two or more Items are Error Flag Marked (C1 Ep).

2) C2 Detection/Revision Section

The data from C1 Detection/Revision Section is De-interleave Processed and sent to C2 Revision Section. Here, only when the ratio of a miss judgement is low, Revision Processing is done.

Because of this, the Cl Ep marks from C1 Revision Section are used as one judgement information in C2 Revision Section. Here upto two High Priority Items are deleted and three or more errors Correction Flag Marked (C2 Ep) and are moved the the Correction Output Mode.

The C1 and C2 Judgement Results are output through the SPDA pin as shown in Diagrams 6-4 and 6-5 and are used as Monitor Signals.

C1 S1	C1 S0	C1 Ep	Judgement Result
0	0	0	No Error
0	1	0	One Error Revised
1	0	1	Two or more Errors, No Revision

Diagram 6-4 C1 Revision Judgement Results

C2 S1	C2 S0	C2 Ep	Judgement Result
0	0	0	No Error
0	1	0	One Error Revised
1	0	0	Two Errors Revised
1	1	1	Three or more Errors Corrected

Diagram 6-5 C2 Revision Judgement Results

• Data Correction Output Circuit

The C2 Revision Processed Data is Scramble Processed (including two delay processing) under CD standards by the external RAM Address Control. This data is consecutively read from the external RAM in Output Word Order from the 8 bit LSB side.

The selection of each data between Direct Output, Average Correction Value Output or Prior Point Hold Output is done in reference to the C2 Ep Correction Mark Flags.

An example of the Correction Process Operation is shown in Diagram 6-10.

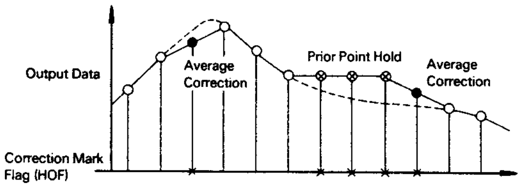


Diagram 6-10 Correction Process Operation Example

Correction Mark Flag (HOF)		Output Data	Output Mode
Dn	Dn+1	Dn	
0	—	Dn	Direct Output
1	0	$\frac{D_{n-1}+D_{n+1}}{2}$	Average Correction Value
1	1	D_{n-1}	Prior Point Hold

Diagram 6-6 Correction Algorithm

Note: When the ~ HOSTP Flag, explained on Page 40, is set to "L", the Correction Operation is stopped and changed to Direct Output Mode.

This flag is very useful when applied to the CD-ROM and CD Information Files.

Also, Correction Flag is added to each word data of the 8-bit LSB side (L-HOF) and 8-bit MSB side (M-HOF) individually and is output through the HOF pin in the order of L-HOF and M-HOF to the Correction Data and output simultaneously.

HOF Correction Alogrythems is set to HOF = 1 if either L-HOF or M-HOF is 1.

CIRCUIT DESCRIPTION

• Attenuator Circuit

During Search, Fast Forward, and Reverse operations in the CD Player, there is a need for an Attenuator Circuit to lower the level of "harmful" sound.

A Fixed Attenuation Level of −12 dB enters from the SCDA pin where it is decided whether to attenuate or not.

Internal switching is done is accordance to the ~ ATT Signal.

When ~ ATT = "L", −12 dB Attenuation

• Muting Circuit

When an abnormal signal enters, it is detected as an Error in the Revision Processing Mode and then eliminated in the Correction Output Circuit. But a certain amount of Bust Error is repeated and that repeated low frequecy sound is output. When a long Bust Error is emitted, the direct current signal, a poor quality sound, is output.

To avoid the just mentioned phenomenon, these signals are passed through the Muting Circuit.

The Muting Operations are explained in the following.

When Muting Operations are started, the Attenuate Circuit (−12 dB) comes ON at the same time, and Zero Cross Detection is done.

The operation for each channel, L and R, are done individually where when the Zero Cross Data (Marked Beat Inversed) is detected, Muting is ON and the digital output data turns to "0".

Muting cancelling is done in the same way.

Control of the Muting Circuit is done with the input command ~ MUTI and MUTC from the SCDA pin.

~ MUTI: Forced Muting Command
When "L", Muting is forced to ON

MUTI: Internal Muting Control Command
When internal "H" is detected, this command stands.

MUTING MODE	SET CONDITIONS	RESET CONDITIONS
64F-Er	When a 64-Frame Burst Error is detected in C1 Revision Mode	When two consecutive revision frames occur in C2 Revision Mode.
DIN-MISS	When a De-interleave Miss occurs three consecutive times.	
BUF-ON	When the Buffer Capacity exceeds ±5 Frames	

Diagram 6-7 Internal Muting Commands

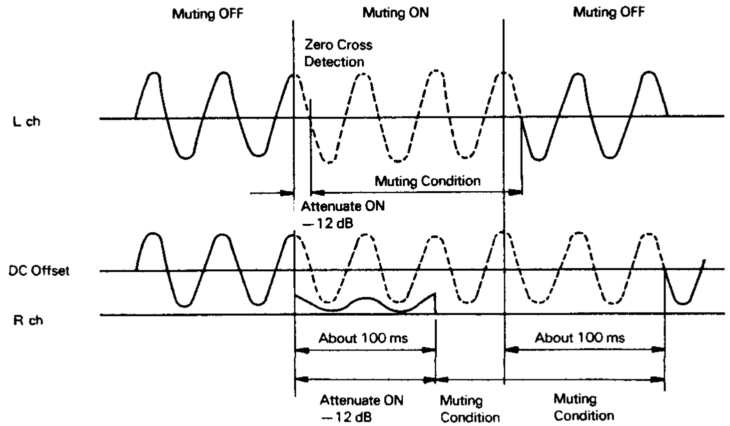


Diagram 6-11 Muting Operation

CIRCUIT DESCRIPTION

• Data Output Circuit

This circuit outputs the input data from the Correction Output Circuit.

The channel data of both L and R, from the MSB side to Beat Serial, are output through the DOUT pin.

All the data output is synchronized with the BCK trailing edge

The signals with connection to the Output Data are shown in the Timing Chart, Diagram 6-12.

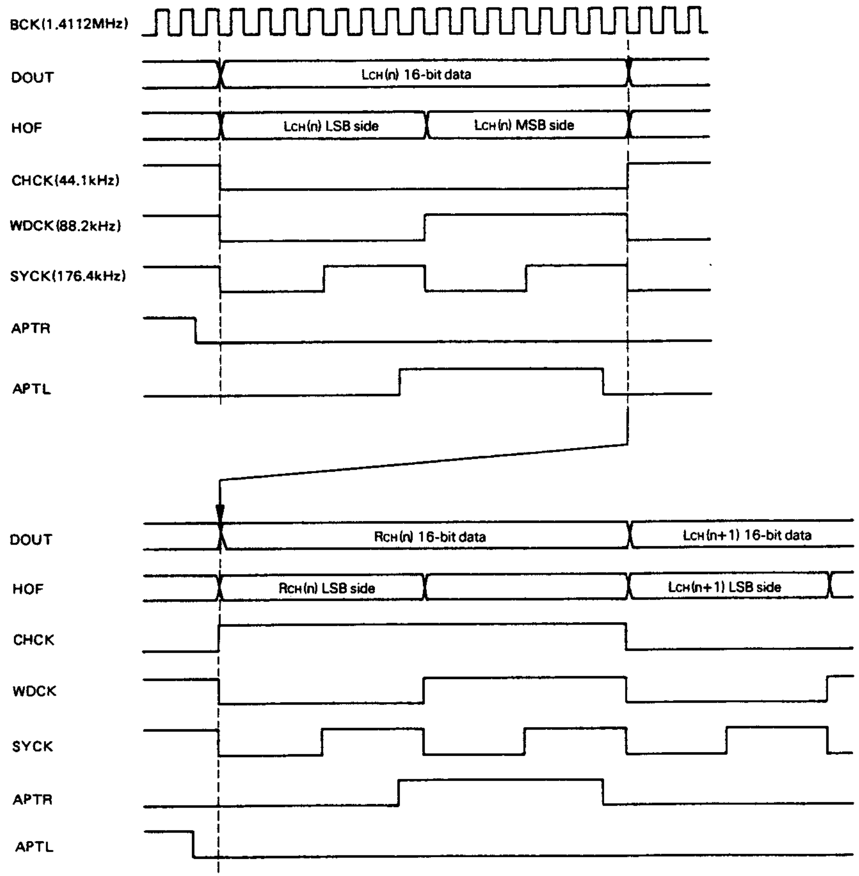


Diagram 6-12 Timing Chart

DP-1510

CIRCUIT DESCRIPTION

• Control Data Input Circuit

Information needed for TC9200BF internal processing is taken in serial mode from the SCDA pin of TC9201BF.

The circuit is designed so that data input, which is in reference with the Revision Mode Synchronizing Signal, COFS (f = 7.35 kHz), is taken in continuously.

Control Data Details:

~ATT: −12 dB Attenuation Command (When "L", Attenuation ON)

~MUTI: Forced Muting Command (When "L", Muting ON)

MUTC: Internal Muting Control Command (When "L", Muting Stop)

~HOSTP: Correction Operation Stop Command (When "L", Correction Operation Stop)

ESGM, ESGL: Selection Signal for setting the times of Off-Synchronized Detection in the Frame Synchronizing Signal Correction Circuit.

WSEG: The Wind Control Signal of the Frame Synchronizing Signa Correction Circuit.

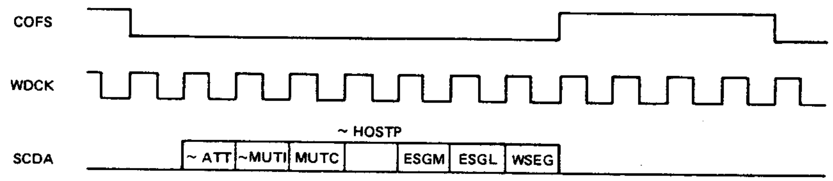


Diagram 6-13 Control Data Input Timing

• Process Status Signal Output Circuit

The Revision Processing Judgement Results and Memory Buffer Capacity Information in TC9200BF is output through th SPDA pin and moved to TC9201BF.

The data output, which is in reference with the Revision Mode Synchronizing Signal, COFS (f=7.35 kHz), is output continuously.

Process Status Signal Details:

FSLO: Complete Synchronized Status Flag (When "L", Complete Synchronized Condition)

FSPS: Synchronized Status Flag (When "L", Synchronized Condition)

MUTO: Internal Muting Detection Flag (When "H", Muting ON)
Note: Will become "H" when 64F-Er., DIN-MISS, BUF-OV on Page 40 occur.

C2 S1-0
C1 C2-0: C1 and C2 Revision Processing Judgement Result

BUF2-0: Memory Buffer Capacity Output Data

DIV+, DIV−: Disc Motor Control Signal

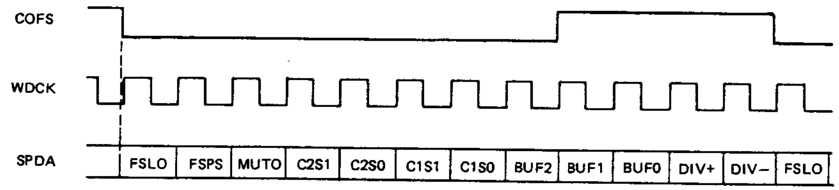


Diagram 6-14 Process Status Signal Output Timing

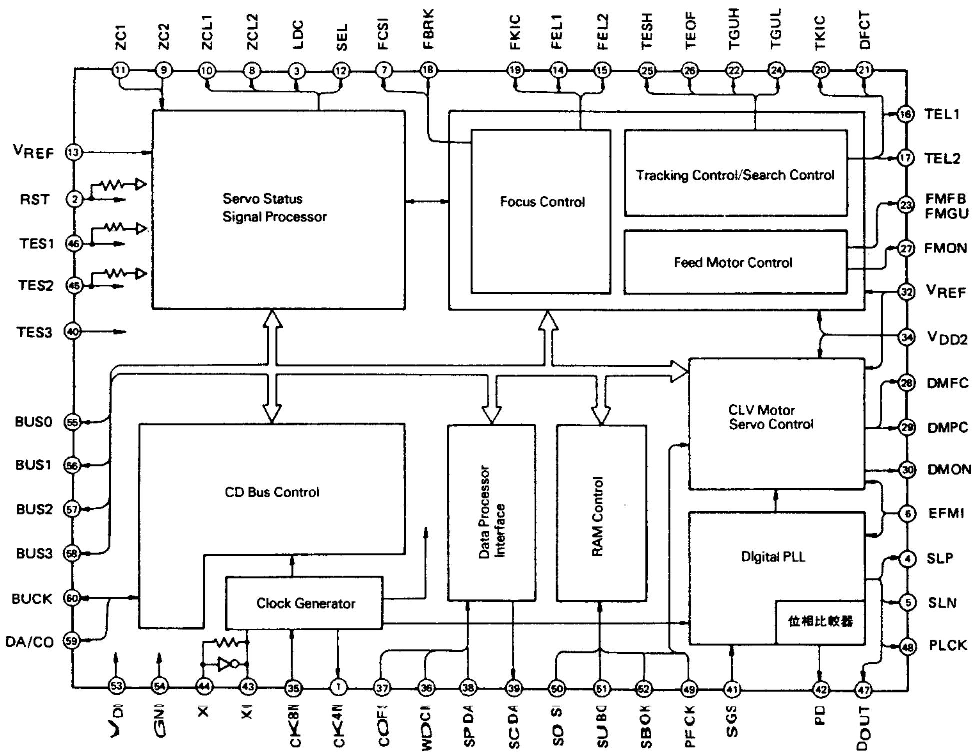
CIRCUIT DESCRIPTION

7. Servo Processor TC9201BF (X32-1400-10:IC)

The TC9201BF is an LSI developed for Pick-up Search and Search Control, Disc Motor CLV Servo Control and MPU incoming/outgoing command interface of the CD Player. When combined with the TA8101N Servo IC (Bi-polar IC) and the TC9200BF Data Processor (CMOS LSI) a simple but powerful Servomechanism can be constructed with the use of very few external components.

- Equipped with an Internal Digital PLL Circuit
- With Four CPU Command Lines, a Clock Line and Acknowledge Line (Total: six lines) all information processing is made possible.
- Automatic Adjustment of Focus and Tracking Gain is made possible.
- The selection of Search Control for Finding Song Beginnings is possible when in any mode.
- Uses the Auto Kick Search Method which is essential for queing and reviewing.
- Equipped with an Internal AFC and APC Circuits for Disc Motor CLV Servo.
- Equipped with an Internal Feed Motor Control Circuit
- Lead Timing is free with the use of a Two Block RAM Buffer for the Subcode Q Data

7.1/ Block Diagram



CIRCUIT DESCRIPTION

7-2. Pin Configuration

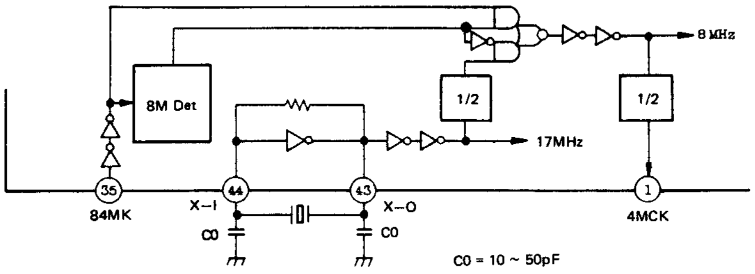
Pin No.	Port name	I/O	Operation
1	4MCK	O	4M Clock Output Pin. f = 4.2336 MHz (X'tal Divided)
2	RST	I	Reset Input Pin. Normally "H" or OPEN (When "L" System Reset)
3	LDC	O	Control Signal Output Pin for the Laser Diode Drive Circuit
4	SLP	O	ELM Signal Direct Input Pin
5	SLN	O	ELM Signal Inverse Output Pin
6	EFMI	I	ELM Signal Input Pin
7	FCSI	O	Focus Actuator Drive Signal Polar Command Output Pin
8	ZCL2	O	Internal DA Converter Output Pin 2
9	ZC2	I	External Comparator Output Signal Input Pin 2
10	ZCL1	O	Internal DA Converter Output Pin 1
11	ZC1	I	External Comparator Output Signal Input Pin 1
12	SEL	O	Pick-up Servo Mode Command Signal Output Pin
13	VR1	—	Internal DA Converter Power Pin. +2.2 V (VREF)
14, 15	FEL1, FEL2	O	Analog Switch for Focus Gain Output Pin
16, 17	TEL1, TEL2	O	Analog Switch for Tracking Gain Output Pin
18	FBRK	O	Focus Actuator Brake Signal Output Pin
19	FKIC	O	Focus Actuator Drive Signal Output Pin
20	TKIC	O	Tracking Actuator Kick Signal Output Pin
21	DFCT	O	Defect Detection Pin. Only in Normal Play from the PU Output Signal Defect is Detected. During Detection VR2 becomes Electric Potential. (Normally: "Hi-Z")
22	TGUH	O	Tracking Servo Loop for Mid and High Range Phase Compensation Mechanism Switching Analog Switch Output Pin
23	VDD	—	Power (+5 V)
24	TGUL	O	Tracking Servo Loop for Low Range Gain Switching Analog Switch Output Pin
25	TESH	I	Tracking Error Signal for Sample Hold Analog Switch Input Pin
26	TEOF	O	Analog Switch Output Pin for Tracking Servo Operation ON/OFF
27	FMON	O	Analog Switch Output Pin for Sending Servo Operation ON/OFF
28	DMFC	O	AFC Output Pin for Disc Motor CLV Servo
29	DMPC	O	APC Output Pin for Disc Motor CLV Servo
30	DMON	O	Analog Switch Output Pin for Disc Motor Drive Circuit Gain Switching
31	FMGU	O	Analog Switch Output Pin for Sending Servo Loop Gain Switching
32	VR2	—	Pick-up Servo Circuit, Disc Servo Circuit Reference Power Pin. +2.2 V (VREF)
33	FMFB	O	Control Signal Output Pin for Feed Motor Forward/Backward Movement
34	VDD2	—	Pick-up Servo Circuit, Disc Servo Circuit Power Pin. 2 × VR2
35	84MK	I	8M Clock Input Pin. f = 8.4672 MHz (X'tal Divided)
36	WDCK	I	Clock Input Pin for Incoming/Outgoing Control Data
37	COFS	I	Revision Mode Frame Synchronizing Signal Input Pin f = 7.35 kHz
38	SPDA	I	Serial Input Pin for Status Signal
39	SCDA	O	Serial Output Pin for Control Data
40	TES3	I	Test Pin (Normally "L")
41	SGS	I	PLL Circuit Selection Pin. When "H" Analog PLL Circuit and "L" Digital PLL Circuit Selection
42	PD	O	Phase Comparison Signal Output Pin for the PLL
43	X-O	O	Crystal Resonator Connection Pin. The Crystal Resonator provides the System with the desired Clock Frequency.
44	X-I	I	Crystal Resonator Connection Pin. The Crystal Resonator provides the System with the desired Clock Frequency.
45, 46	TES2, TES1	I	Test Pin (Pull-up Resistor included) Normally "H" or OPEN
47	DOUT	O	EFM Signal Output Pin
48	PLCK	O	Bit Clock Output Pin

Pin No.	Port name	I/O	Operation
49	PFCK	I	Play Mode Frame Synchronizing Signal Input Pin. SUBQ, SBOK and S0 S1 are synchronized to the fall edge of this signal and input. Also, the compared frequency of the AFC and APC are used for the CLV Servo.
50	S0 S1	I	Sub-code Signal Synchronizing Pattern S0 and S1 Input Pin
51	SUBQ	I	Sub-code Signal Q Data Input Pin. 80-bit Q Data as one block is serial input, and saved in the internal RAM.
52	SBOK	I	Sub-code Signal CRC Check Judgement Result Input Pin. (Normal = "H", Error = "L")
53	VDD	—	Power (+5 V)
54	Vss	—	GND Pin
55~58	BUS0~BUS3	I/O	Incoming/Outgoing Command and Data Bus Line. With the BUCK Start-up, the Command and Data is internally released. Also during BUCK "H", the input data is output on the Bus.
59	DA/CO	I/O	Control Input/Output Pin for Command and Data Processing. When the MPU sends a One-Word Item Command, the Pin is "L" (Input). When all the Command and Data has been correctly received and while BUCK is "L", the pin is "L" (Output). This is then used as the MPU Acknowledge (ACK) Signal (Normally "H").
60	BUCK	I	Clock Input Pin for the Incoming/Outgoing Command and Data. During Reception the "L" period will be more than 9 μs, and "H" period will be more than 4 μs while less than 90 μs. 4 μs after BUCK Start-up, DA/CO and BUS0-3 will be switched.

7-3. Operation Information

• Timing Producing Circuit

The Timing Producing Circuit creates the clock frequency needed for internal operation (Master Clock is 8 MHz). The input conditions to the 84MK pin, as shown in Diagram 10-1, is internally switched whether to use the 84MK input or (X-I)/2 as the Master Clock by checking the 8M Det.



Note: Use a crystal with low CI values for best Start-up Conditions

Diagram 7-1

SGS Pin	84MK Pin	X-I Pin	4MCK Output Pin	Notes
L	L	16.9344 MHz	X-I/4	Digital PLL ON
	8.4672 MHz	17.2872 MHz	84MK	
H		8.6436 MHz	2	Analog PLL ON

Diagram 7-1 Internal Clock Selection Mode

• CPU Interface Circuit (CD Bus Control Circuit)

The CD Bus Control Circuit was designed so that the connection between the general purpose 4-bit CPU and the TC9201BF could be easily achieved so that data communication could be done through only six lines, four line of the I/O Data Bus (BUS 0-3), the Clock Line and the DA/CO line (for the Data and Command Differential Signal).

The Bus Line conditions for the three modes, Idle Mode and the Read/Write Modes, are explained in the following 1) ~ 3).

Before this though, the following points must be noted about the CD Bus and Data Communications between the CPU and TC9201BF.

1 Only the CPU will output the BUCK.
2 The level of the BUCK will be "H" when there is no data being communicated.
3 The period of "H" level of the BUCK will be less than 90 μs while data is being transmitted from the CPU.
4 The BUS 3-0 Input Data should be delayed by more the 4 μs in reference to the BUCK trailing edge.
5 The BUS 0-3 and DA/CO pins should be an Open Drain CPU with Wired OR functions or Open Collector Type CPU with an I/O port.
6 The transmission/reception of one word (4 bits) data is to be done with the period from the current trailing edge to the next one.

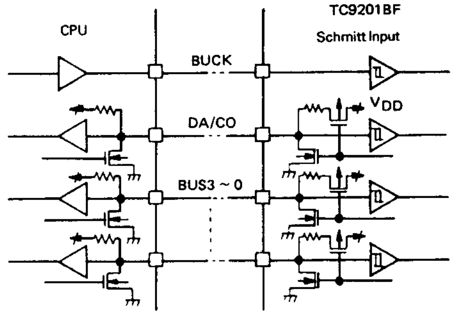


Diagram 7-2 BUS Line Input/Output Construction

1) Idle Mode

This is the mode when there is no commmunications being done with the CPU. In this mode both the BUCK and DA/CO pin have an "H" level while the internal conditions for the Monitor Signal are being emitted through BUS 0-3. From BUS 0, "H" level, from BUS 1, AFCS, from BUS 2, QDRE, and from BUS 3, FOK external signals are to be output.

- AFCS Signal ..... CLV Servo Mode Switch Signal (In Main Servo Mode, AFCS = "H" Level)
- QDRE Signal..... Sub-Code Q Data Lead Enable Signal (In Lead Enable, ODRE = "L" Level)
- FOK Signal ...... Focus ON/OFF Judgement Signal (in Focus ON, FOK = "H" Level)

See other reference documents for details of each of the above mentioned signals.

In Idle Mode, when either BUS 2 or 3 are "L" Level (Sub-Code Q Data Lead Enable or Focus OFF), DA/CO Line will be "L" level. This means that the TC9201BF will break into the Idle Mode when DA/CO is "L" level. It is possible to make a smooth recovery when becomes FOK = "L" (Focus OFF).

CIRCUIT DESCRIPTION

2) Write Command Input Mode
This mode transmits the Write Command and Four-Word Data (CM-A)-(CM-D) from the CPU to TC9201BF. The first two words are Commands (C6 ~ C0) and the next two words are the Data (D7-D0).
TC9201BF takes in the Command or Data of the BUS from the BUCK trailing edge and will then Echo Back the content on the BUS when BUCK is "H". Therefore, it is possible to confirm whether the Command or Data has been correctly received by checking the BUS 0-3 condition at BUCK Trailing Edge (since the BUS line is Wired OR, Error Detection during "L" is not possible).
When a Write Command is input, it is synchronized to the BUCK trailing edge (Actually, the DA/CO and the CPU information is delayed by 4 μs after the BUCK trailing edge.
The same delay is needed in the Lead Command Input)
Also, when a Write Command is input, the first word of the command BUS 3 is "H" level, while the DA/CO line becomes "L" (Command Transmission Start). When the second Command and Data word are correctly received, TC9201BF will return the ACK acknowledge signal, on the DA/CO Line (when the Write Command is correctly input and reception is complete, DA/CO Line is "L" Level). When this ACK is returned, the BUS line switches from Command Input Mode to Idle Mode again.
If the ACK is not returned, this means that there is Reception Error, so the Command is sent again. This is same for a Read Command too.

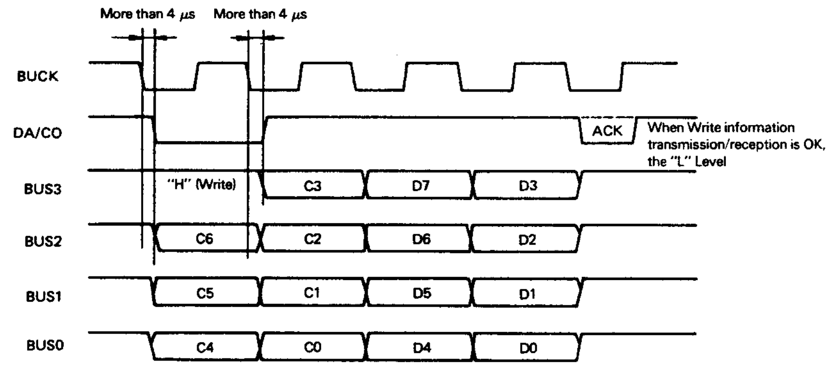


Diagram 7-3 Write Command Input Example

DP-1510

CIRCUIT DESCRIPTION

3) Read Command Input Mode
In this mode, when a one-word Read Command (SQRD and STRD Command) from the CPU is transmitted, TC9201BF sends the designated data back through the BUS line. The handling of the BUCK and Commands are same as in Write Mode, but in Read Mode, but when a command is input, BUS 3 line is "L" level while the DA/CO line is "L" level at the same time. Therefore, whether the first word on the BUS 3 line is "H" or "L" differentiates between a Write and Read Command.
When the transmission/reception of the desiganated data is complete, an ACK signal is returned to the CPU where the BUS line then switches to Idle Mode.

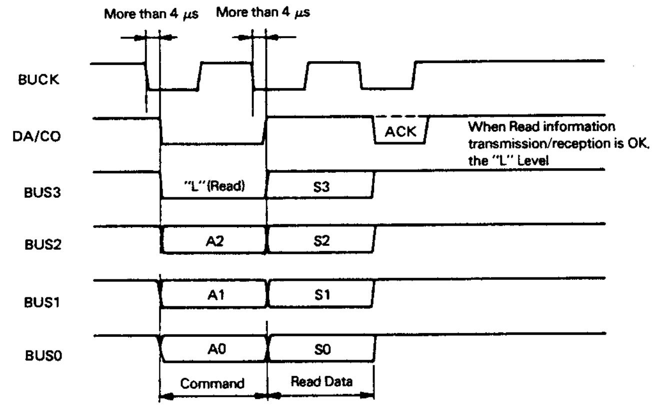


Diagram 7-4 Read Command Input Example

4) Control Command Details

(1) Write Command (CM-A)

COMMAND	HEX	CODE C7	C6	C5	C4	C3	C2	C1	C0	PROCESSING DETAILS	CONDITIONS
SDSET	80	1	0	0	0	0	0	0	0	While Focus OFF, Sub-beam Summing Data is to latched to SB-REG	
PUSTP	81	1	0	0	0	0	0	0	1	Operations of PUFWD and PUBWD are stopped. (Sending Servo and Tracking Servo are turned OFF)	
PUFWD	82	1	0	0	0	0	0	1	0	Pick-up is moved in a forward direction (PU)	
PUBWD	83	1	0	0	0	0	0	1	1	Pick-up is moved in a backward direction (PU)	
LDON	84	1	0	0	0	0	1	0	0	Laser Diode is turned ON (LD).	
LDOFF	85	1	0	0	0	0	1	0	1	Laser Diode is turned OFF (LD).	
DMSV	86	1	0	0	0	0	1	1	0	CLV Servo of the Disc Motor is turned ON.	FOK (Focus ON)
DMOFF	87	1	0	0	0	0	1	1	1	CLV Servo of the Disc Motor is turned OFF. DMBK and DMFK are cancelled.	
FGASS	88	1	0	0	0	1	0	0	0	FKIC Output is set to "H" level.	LDON
FGASR	89	1	0	0	0	1	0	0	1	FKIC Output is set to "L" level.	LDON
FGASET	8A	1	0	0	0	1	0	1	0	The data of the internal resistor is decoded and set to FEL1 and 2.	LDON
TGASET	8B	1	0	0	0	1	0	1	1	The data of the internal resistor is decoded and set to TEL1 and 2.	FOK·DMSV
TGASR	8C	1	0	0	0	1	1	0	0	TKIC Output is set to "L" level	FOK·DMSV
TGASS	8D	1	0	0	0	1	1	0	1	TKIC Output is set to "H" level	FOK·DMSV
FOSET	8E	1	0	0	0	1	1	1	0	FCSI Output is set to "H" level	LDON
FORST	8F	1	0	0	0	1	1	1	1	FCSI Output is set to "H" level	LDON

Notes:
- In CM-A, there is no need for data. D0~D7 = (XXXX XXXX)
- After running CM-A, Tracking Servo and Sending Servo are turned OFF.

(2)/ Write Command (CM-B)

COMMAND	HEX	CODE C7	C6	C5	C4	C3	C2	C1	C0	PROCESSING DETAILS	CONDITIONS
ATTON	92	1	0	0	1	0	0	1	0	TC9200BF − 12 dB Attenuate is turned ON	
ATTOFF	93	1	0	0	1	0	0	1	1	TC9200BF − 12 dB Attenuate is turned OFF	
MUTON	94	1	0	0	1	0	1	0	0	TC9200BF Muting is turned ON	
MUTOFF	95	1	0	0	1	0	1	0	1	TC9200BF Muting is turned OFF	
DMBK	96	1	0	0	1	0	1	1	0	Forced Reverse Torque of the Disc Motor is applied.	DMSV
DMFK	97	1	0	0	1	0	1	1	1	Forced Speed-up Torque of the Disc Motor is applied.	LDON·DMSV

Notes:
- In CM-B, there is no need for data. D0 ~ D7 = (XXXX XXXX)
- During Reset (RST = "L", ATT = "OFF" and MUTE = "ON" are set.

(3) Write Command (CM-C)

COMMAND	HEX	CODE C7	C6	C5	C4	C3	C2	C1	C0	DATA D7	D6	D5	D4	D3	D2	D1	D0	NOTES
SETRO	98	1	0	0	1	1	0	0	0	ATTC	MUTC	HOSTP	GUPCL	MCG	FSPS	DIV+	DIV−	
SRCK	99	1	0	0	1	1	0	0	1	SRCK				×	×	×	×	SRCK: Through Rate Clock Switching Data
FOCUS	9A	1	0	0	1	1	0	1	0	FS				FCOK				FS: Focus Stand-by Level FCOK: Focus OK Level
DEFECT-I	9B	1	0	0	1	1	0	1	1	N				TN				N: Scratch Detection Level TN: Mono/Multi Time Constant
DEFECT-II	9C	1	0	0	1	1	1	0	0	M				TM				M: Scratch Detection Level TM: Mono/Multi Time Constant
SHOCK	9D	1	0	0	1	1	1	0	1	L				TL				L: Shock Detection Level TL: Mono/Multi Time Constant
SETR 1	9E	1	0	0	1	1	1	1	0	1	APCG 1	APCG 2	WSEG	ESGL	ESGM	1	DMG	
SETR 2	9F	1	0	0	1	1	1	1	1	GUP 1	HYS 1	GUP 2	HYS 2	LDCP	RFRG 1	RFRG 2	FMSS	

CIRCUIT DESCRIPTION

Details (Data D7 ~ D0)

1 SETRO

- ATTC: Attenuate Control Signal for CKIC and CKICF (During Continuous Kick)
  - When "1" during Continuous Kick, ATT is ON.
- MUTC: TC9200BF Internal Muting Control Command
  - Normally "1"
  - When "0", Internal Muting is OFF.
  - Sent to TC9200BF
- HOSTP: TC9200BF Correction Operation Stop Command
  - Normally "1"
  - When "0", Correction Operation is stopped.
  - Sent to TC9200BF
- GUPCL: Clear Control Signal for the Gain Up (GUP) Signal during Shock Detection
  - DEFECT Signal is cleared when GUP is "1".
  - DEFECT Signal is not cleared when GUP is "0".
- MCG: FSPS, DIV+ and DIV– Selection Signal
  - When "1", CPU combined information used from TC9178AF and during TC917F System operation
  - When "0", SPDA information sent from TC9200BF is used.
- FSPS
- DIV+ : CLV Servo System Control Information
- DIV–

2 SETR1

- APCG1 APC Phase Comparison Frequency Selection
- APCG2 Signal of the CLV Servo Circuit

APCG 1	APCG 2	PHASE COMPARISON FREQUENCY	DIVISION COMPARISON
0	0	1225 Hz	7.35 kHz/6
1	0	919 Hz	7.35 kHz/8
0	1	613 Hz	7.35 kHz/12
1	1	459 Hz	7.35 kHz/16

- WSEG: Wind Selection Signal for the TC9200BF Frame Synchronizing Signal Protection Circuit
  - Sent through the SCDA pin to TC9200BF

WSEG	WIND WIDTH
1	±7
0	±3

- ESGM Circuit Setting Selection Signal for the TC9200BF
  : Frame Synchronizing Signal Protection Circuit for
- ESGL Continuous Off-Synchronizing Detection
  - Sent through the SCDA pin to TC9200BF

ESGM	ESGL	NUMBER OF OCCURANCES
1	1	2
1	0	4
0	1	8
0	0	12

- DMG: DMON pin Control Signal
  - When "1", during DMSV (CLV Servo ON) DMON = VREF
  - When "0", during DMSV (CLV Servo ON)
    If AFCS = 1 then DMON = "HiZ"
    If AFCS = 0 then DMON = "VREF"
  AFCS = 1 → Pre Servo Mode
  AFCS = 0 → Main Servo Mode

3 SETR2

- GUP1: When "1", Gain Up of the Tracking Servo during Shock Detection while Playing
- HYS1: When "1", Tracking Signal is to have Hysteresis Characteristics during Shock Detection while Playing
- GUP2: When "1", Gain Up of the Tracking Servo for 2-3 msec after Search completed.
- HYS2: When "1", Tracking Signal is to keep Hysteresis for 2-3 msec after Search completed.
- LDSP: When "0", LDC pin is "HiZ" during LDON (Same during Reset)
- RFRG1/2: RF Wipe Off Level Selection Signal

RFRG 1	RFRG 2	WIPE OFF LEVEL
0	0	01111
1	0	01110
0	0	01101
1	1	01100

- FMSS: When "0", Feed Servo OFF during Search Normally "1"

CIRCUIT DESCRIPTION

(4) Write Command (CM-D)

COMMAND	Hex	CODE C7	C6	C5	C4	C3	C2	C1	C0	DATA D7	D6	D5	D4	D3	D2	D1	D0	NOTES
PAUSE	A×	1	0	1	0					Number of Tracks N1								
FEED	B×	1	0	1	1					Number of Tracks N2								64 × N2 Track Kick
NKIC	C×	1	1	0	0	BRK	FGC	TGC	B/F	Number of Tracks N1								N1 Track Kick
NKICF	D×	1	1	0	1					Number of Tracks N1								N1 Track Kick (Feed Motor Sending Included)
CKIC	E×	1	1	1	0					×	×	T		Number of Tracks N3				N3 Continuous Track Kick T: Speed Select
CKICF	F×	1	1	1	1					×	×	T		Number of Tracks N3				N3 Continuous Track Kick (Feed Motor Sending Included) T: Speed Select

Details

- BRK: Feed Motor Brake Signal ON/OFF Setting
  - When "1", Brake Signal ON
  - When "0", Brake Signal OFF
- FGC: Feed Motor Gain Control
  - When "1", FMGU pin is "VREF" (Gain Up).
  - When "0", FMGU pin is "Hiz".
- TGC: Tracking Motor Gain Control
  - When "1", TGUL and TGUH pins are "HiZ" (Gain Up)
  - When "0", TGUL and TGUH pins are "VREF"
- B/F: BWD/FWD Search Direction Setting
  - When "1", BWD Search
  - When "0", FWD Search
- N1: Number of Kick Tracks (8 bits) — Kick Amount = N1 Track (0-255)
- N2: Number of Kick Tracks (8 bits) — Kick Amount = 64 × N2 Track (0-16320)
- N3: Number of Kick Tracks (8 bits) — Kick Amount = N3 Track (0-15)
- T: Kick Interval (2 bits) during CKIC and CKICF

T (D5)	T (D4)	KICK INTERVAL
0	0	62 ms (16 Hz)
0	1	124 ms (8 Hz)
1	0	248 ms (4 Hz)
1	1	495 ms (2 Hz)

(5) Read Command (CM-E)

COMMAND	Hex	CODE C3	C2	C1	C0	DATA D3	D2	D1	D0	NUMBER OF WORDS READ	NOTES
SQRD	0	0	0	0	0	QDa	QDb	QDc	QDd	20	Sub-code Q Data Read Command QDa = MSB
STRD	1	0	0	0	1	FOK	QDRE	SRCH	BRKR	1	Internal Status Monitor Command

Details

STRD

- FOK: Focus Search OK Signal
  - When "H", Focus ON (Servo ON)
- ODRE: QData Read Enable Signal
  - When "L", Enable
- SRCH: Search Signal
  - When "L", Searching
- BRKR: Disc Motor Brake Cancel Signal
  - When "H", Brake Cancelled

CIRCUIT DESCRIPTION

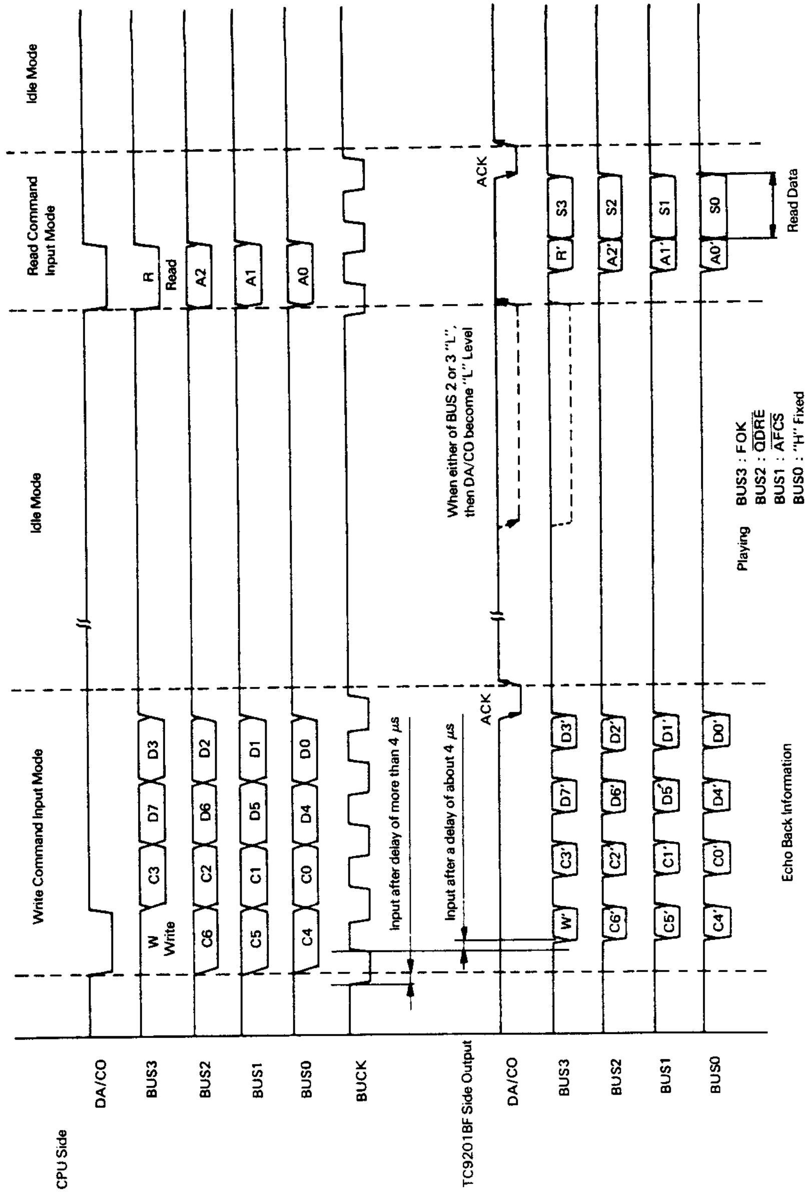


Diagram 7-5 CPU Circuit Timing Chart

CIRCUIT DESCRIPTION

- **PLL Circuit**

TC9201BF is equipped with an Analog and a Digital PLL Circuit As shown in Diagram 7-1 on Page 43, there are three modes. Switching of these modes is done by using the SGS pin and 84MK pin.

There is an internal correction circuit for phase deviation in the EFM for such reasons as Disc Memory Accuracy and when the Disc is Off Center. This is very useful, especially when using the digital PLL. Therefore, this lets the Slice Level of the Data Slicer be fixed (AC center). The Analog PLL cannot be used for this though.

1) Analog PLL Circuit

When SGS is set to "H" level (input of X'tal 8.4672 MHz Clock from the 84MK pin), the Analog PLL Mode comes into operation.

The Block Diagram of this is shown in Diagram 7-6 and the Timing Chart in Diagram 7-7.

Also, the PLCK Phase Polar Differential Signal, in reference to the EFM Signal Trailing/Leading Edge, is output in tri-state form the PD pin after passing the Change Pump.

As mentioned before, the Timing of the Analog PLL Circuit is shown in Diagram 7-7. Here the DOUT output EFM signal is data that has been delayed after being straightened out in PLCK.

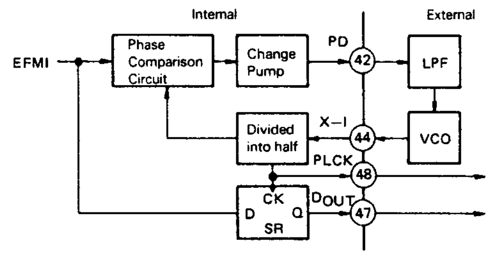


Diagram 7-6 Anaolog PLL Block Construction

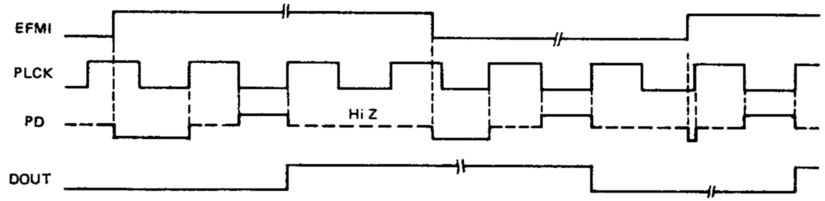


Diagram 7-7 Analog PLL Timing

2) Digital PLL Circuit

When the SGS pin is set "L", the Digital PLL Circuit comes into operation. With this, two frequencies are available, 16.9344 MHz and 17.2872 MHz (4.3218 MHz from the EFM Input Signal Beat Rate × 4). The use of these two crystal frequency modes is done either by inputing into the 84MK 8.4672 MHz (16.9344 MHz/2) or fixing 84MK with "L" level.

This Digital PLL Circuit has a unique construction where it not only measures its own efficiency but also requires no external components. Also, since the Lock Range and Capture Range are about ±1%, the Disc Mode, from the CLV Servo, Speed Range needs to be kept within ±1%.

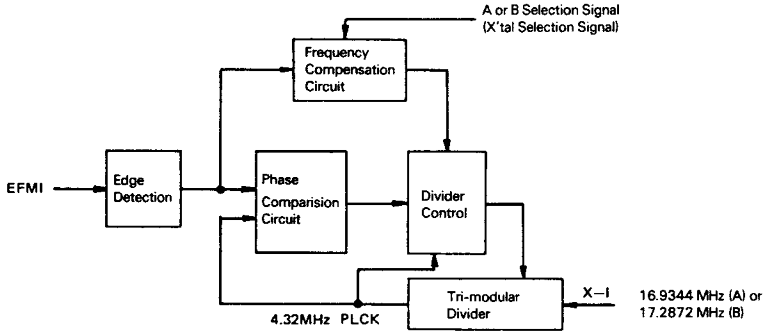


Diagram 7-8 Basis Block Digital PLL Circuit Construction

The operations of the Digital PLL Circuit are as follows:

1 Edge Detection of the EFMI input is done and passed to Phase Comparison Circuit
2 In the Phase Comparison Circuit the phase difference between the EFMI Edge and PLCK are detected after being resolved with $\pi/4$ (as shown in Diagram 7-9).
3 With the Phase Polar Difference Information detected in the Phase Comparison Circuit, the Tri-modular division difference is controlled thus controlling the phase difference to the least possible.

The Tri-modular Divider is able to compare 1/4-0.5, 1/4 and 1/5-0.5 divisions. The division difference control of the divider will be done only when the Phase Difference Information is within ±2 as shown in Diagram 7-9.

Since the Clock Frequency of 16.9344 MHz, input through the X-I pin, will differ from four times the Beat Rate of the EFMI input (4.3218 MHz × 4 = 17.2872 MHz), Frequency Compensation is required.

Therefore, when the Edge Detection Period of EFMI is $T_P \leqq 6T$ (1T = 1 PLCK) division difference control of the divider will be done; and when $T_P \geqq 6T$, then Edge Detection of EFMI and a 6T period is controlled. By doing this, the system is stabilized.

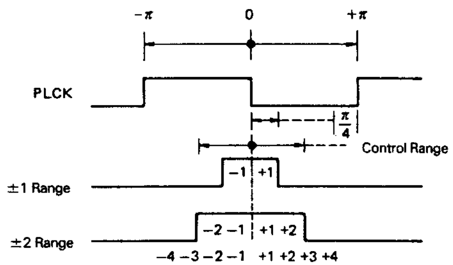


Diagram 7-9 PLCK Division

3) Data Slice Level Correction Circuit

The Slice Level of the Data Slicer is normally takes the DC content out of the Data Slice Output from the ELM signal and feeds this back. The aim of the Data Slice Level Correction Circuit is to fix this Data Slice Level and make no adjustment needed possible.

Therefore, the Data Slice Correction Circuit takes the phase deviation that occurs from the Memory Accurancy of the Disc, when the Disc is Off Center and from Disc Motor Jitter when the Slice Level is fixed and passes it through the Phase Detection Circuit. Corrections are made in reference to the Phase Differential Information detected.

In this case, the phase deviation usually occurs in low range frequencies. Therefore, as shown in Diagram 7-10, even when the Slice Level varies vertically, the distance between EFMI Leading Edge to Leading Edge or Trailing Edge to Trailing Edge does not change.

This means that when $T_A = T_B = T_C$, as shown in Diagram 7-10, T_A is the reference where after this the slice level variation can be easily detected in T_B and T_C. It is then possible to reconstruct the original data in the D_{OUT} Correction Output Circuit with the detection results.

This means that when the Digital PLL Circuit in TC9201BF is used, not only will the there be no need to use the Analog Slice Level Control but the Slice Level Response will become extremely accurate with much less data errors.

Note that the Slice Level Correction Range is less than ±2T (1T=1PLCK)

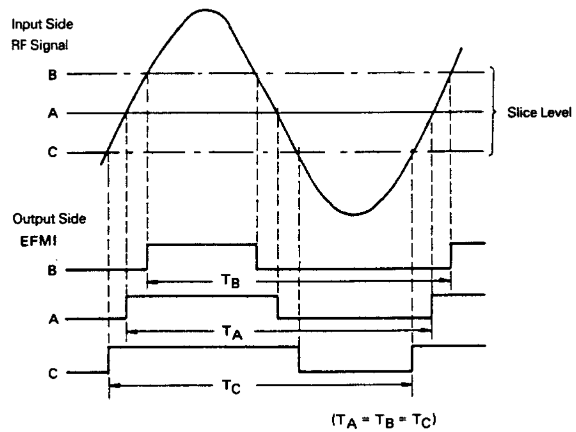


Diagram 7-10 Data Slicer Input/Output Waveform

●CLV Servo Circuit

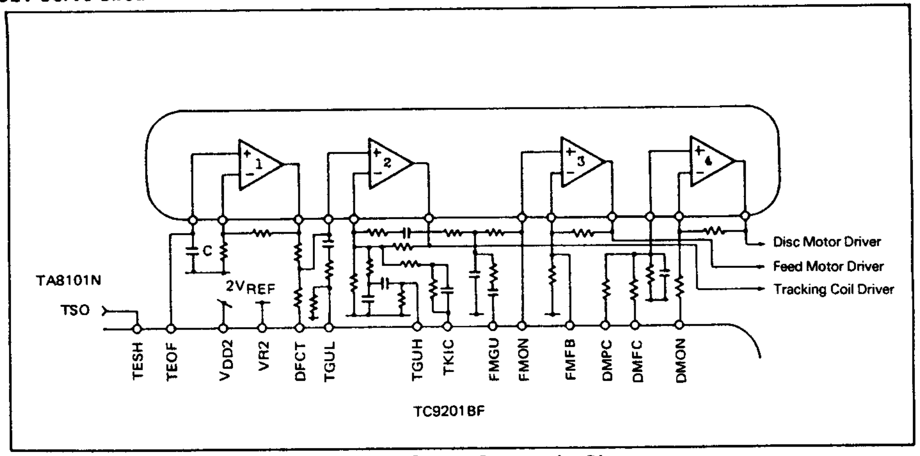


Diagram 7-11 System Construction Diagram

- Correlation
  Pins: DMPC, DMFC, DMON
- Commands: DMSV (86xx), DMOFF (87xx), DMBK (96xx), DMFK (97xx), SETRO (98R1R2), SETR1 (9ER3R4), STRD (1)

Command Reception Conditions

COMMAND	RECEPTION CONDITION	OPERATION
DMSV	FOK=H (Focus ON)	CLV Servo ON
DMOFF	—	Disc Motor Stop
DMBK	DMSV Command Set	Disc Motor Brake
DMFK	LDON Command Set*	Disc Motor Speed Up

* **When the DMSV Command is not operating, DMFK Command is used.**

Note: Each Command Information (Information Details are shown in (CM-C))

DATA	R1	R2	R3	R4
D3	ATTC	MCG	1	ESGL
D2	MUTC	FSPS	APCG1	ESGM
D1	HOSTP	DIV+	APCG2	1
D0	GUPCL	DIV−	WSEG	DMG

The system is designed so that the AFC and APC information needed for the Disc Motor is acquired from the Pre Servo Mode and Main Servo Mode which are divided on the CLV Servo Board.
Actual operation/timing examples shown in Diagrams 7-12 ~ 14.

MODE DIVISION	MODE CONDITIONS	DMPC OUTPUT	DMFC OUTPUT	DMON OUTPUT		NOTES
				DMG DATA		
				0	1	
Pre Servo	AFCS = H Tracking Servo OFF	Tmax Info. Double value output "H" or "L"	PWM Output AFC2 Circuit ON	VREF Fixed	HiZ	During Input of 1 DMSV Command 2 DMFK Command 3 DMBK Command
Main Servo	AFCS = L Tracking Servo ON	Phase Polar Info Tri-state Output	PWM Output (AFC1 Circuit ON)	VREF Fixed		During Input of NKICO Command (Play Command)

Diagram 7-2 CLV Servo Mode Division

V_{REF} = +2.2 V

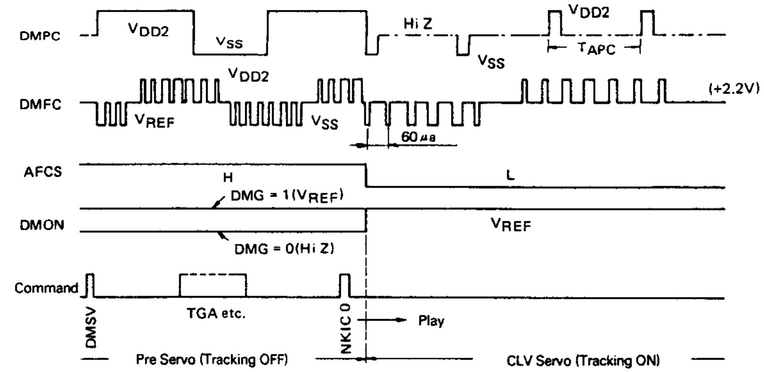


Diagram 7-12 CLV Servo Timing Example 1 (During DMS Command Input)

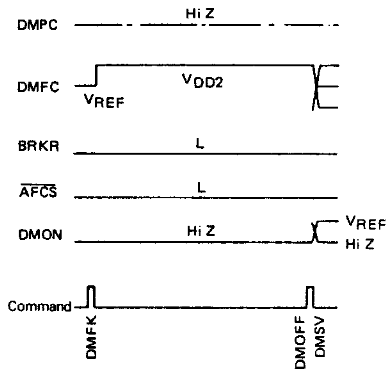


Diagram 7-13 CLV Servo Timing Example 2 (DMFK Command Input)

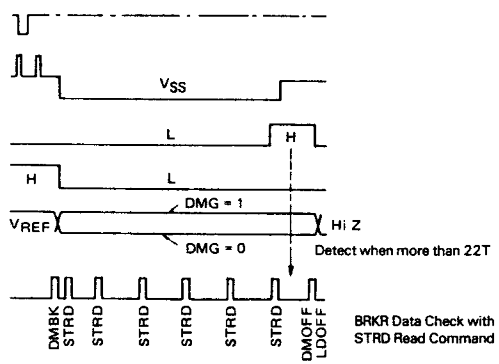


Diagram 7-13 CLV Servo Timing Example 3 (DMBK Command Input)

The following is an explanation of the Pre Servo Mode and the Main Servo Concept.
Details about the CLV Servo Operations will be explained in Items 1) ~ 4) about AFCS, AFC, APC and Brake Cancel Signal Producing Circuits.

- Pre Servo Mode
  When the DMSV Command (CLV Servo ON) is input, after the Focus has be achieved, the Disc Motor will start to revolve.
  Pre Servo Mode takes the turning speed (Frequency Range) to within the Digital PLL Capture Range (about ±1%)
- Main Servo Mode
  When the NKICO Command (Play Command) is input, after the tracking gain adjustment is complete with the Pre Servo Mode conditions, both the Tracking Servo and Feed Motor Servo come ON.
  When the Tracking Servo comes ON, the Synchronized Division Circuit will start and the AFCS will switch from "H" to "L" level, thus going into Main Servo Mode.

CIRCUIT DESCRIPTION

1) AFCS Signal Producing Circuit

AFCS is the switch to Servo Mode. When the AFCS receives the FSPS for the SPDA pin of the TC9201BF or the SETRO Command from the CPU is input, the Mode is switched. Also, the FSPS Signal informs whether the Synchronized Division Circuit is in operation thus turning the Tracking Servo ON and if the EFM Signal has Phase Locked, it will maintain an "L" level.
The conditions for AFCS to switch between "H" and "L" level are shown in Chart 7-3.

Conditions for AFCS to switch from "H" to "L"	Conditions for AFCS to switch from "L" to "H"
When FSPS "L" level continues for 16 frames	When FSPS "H" level continues for 64 frames

Chart 7-3 AFCS Switch Conditions

2) AFC Signal Producing Circuit

The use of either AFC1 or AFC2 Circuits is decided in Main Servo and Pre Servo Mode. Each mode detects the Frequency Control Signal (AFC) required, as a result of this detection, outputs the PWM wave from the DMFC pin. This PWM wave controls the Disc Motor speed.
The following explains the AFC1 and AFC2 Circuits operations.

1 AFC1 Circuit: (Main Servo Mode, AFCS = L, Synchronized Division Circuit is in operation)

The AFC1 Circuit divides the PFCK (Play Mode 7.35 MHz) by four, and uses this frequency content to detect the X'tal 2.1168 MHz. When the Disc Motor is correctly locked, PFCK/4 = 1152 Clock. The system is designed to keep the Frequency Control Range within about ±5% in TC9201BF.
As shown in Diagram 7-16, in the Frequency Content Detection Circuit, the PFCK/4 (Disc Motor Frequency Information) frequency content is passed to a PWM wave that has 7-bit resolution and then output through the DMFC pin.
Here, the DMFC pin output consists of three values, V_{DD2} ($2V_{REF}$), V_{SS}(0 V) and V_{REF} (+2.2 V).

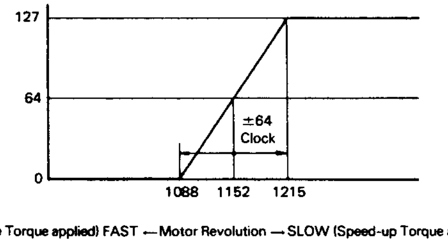


Diagram 7-15 CLV Servo Frequency Control Range

CIRCUIT DESCRIPTION

2 AFC2 Circuit: (Pre Servo Mode, AFCS = H, Synchronized Division Circuit is not in operation)

The AFC2 Circuit uses X'tal 8.4672 MHz from Tmax (Longest Inverse Level Value) from the EFM.
When one clock (4.3218 MHz) is equal to 1T, during Disc Motor Correct Revolution, the Frame Synchronizing Pattern is 11T + 11T = 22T. This is Tmax (Longest Inverse Level Value).
When Tmax is used with X'tal 8.4672 MHz to detect, 22T is equivalent to 43 Clock. When the Detection Result is more than 43, "Disc Motor Revolution Speed SLOW", and when less than 43, "Disc Revolution Speed FAST" is the information passed on.
During Pre Servo Mode, Tmax Q is directly output from the DMPC pin while the 7-bit resolution of the PWM wave is output from the DMFC pin at the same time. Here, the DMFC pin output consists of three values, V_{DD2} ($2V_{REF}$), V_{SS} (0 V) and V_{REF} (+2.2 V).

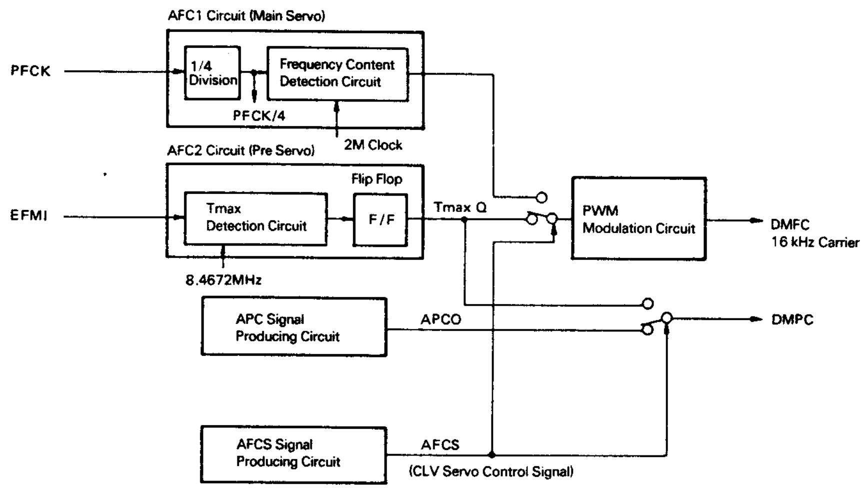


Diagram 7-16 AFC Signal Producing Circuit Block Diagram

3) APC Signal Producing Circuit

This circuit only moves with the Main Servo where the produced APC signal is output in Tri-state from the DMPC pin to control the speed of the Disc Motor.
The APC Signal is the Phase Differential Information of the N Division Signal and the X'tal Signal produced from the Reference Frequency Signal (X'tal Division 7.35 kHz). This Phase Differential Information is output from the DMPC pin. Therefore, as shown in Diagram 7-17, when the PFCK/N is delayed in reference to XFS/N, "H" level is output, and when faster, "L" level is output.

N Division is the data from APCG1 and G2 (set by the SETR1 Command) and can be selected in four values. Select the most accurate value for the CLV Servo from the operation results.
Also, XFS is a division of 2.1168 MHz by 288 times and is controlled to within ±1 with the two data outputs from DIV+ and DIV−. DIV+ and DIV− (Output from the SPDA pin) are the Buffer Memory Status Signals of the external RAM of TC9200BF. The Disc Motor Jitter is corrected and the most accurate conditions is taken to the Buffer here.

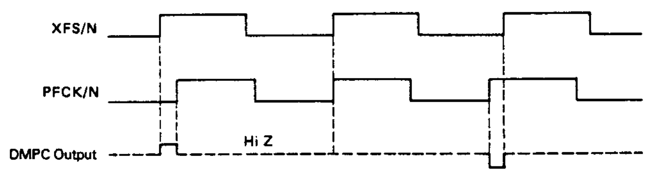


Diagram 7-17 APC Signal Output Timing

APCG 1	APCG 2	N	Phase Comparison Frequency
0	0	6	1225 Hz
1	0	8	919 Hz
0	1	12	613 Hz
1	1	16	459 Hz

DIV+	DIV−	Division Comparison	Disc Motor Revolutions
0	0	1/288	
1	0	1/287	Disc Motor Revolution will become faster.
0	1	1/289	Disc Motor Revolution will become slower.
1	1	1/288	

Note: DIV+ and DIV− can also be input with the SETR0 Command from the CPU.

4) Brake Cancel Signal Producing Circuit

When the DMBR Command is input from the CPU, "L" level becomes fixed from the DMFC pin output and the Disc Motor will be braked. After braking and the Disc Motor revolution speed is slowed, this is detected and the Brake Cancel Signal, BRKR ("H" level), is emitted. The BRKR emission condition is when the ELM Signal Period continues for 512 periods and more than 22T (about 200 kHz) must be achieved. BRKR emission is checked through BUS0 line with the input of the STRD Read Command from the CPU.

• Focus/Tracking Servo Circuit

Basically, TA8101N operates the Three-Beam Pick-up Detection Signal AMP and TC9201BF does all the control of the Focus/Tracking Servo and Tracking Search.

1) Servo Status Signal Processor

The Servo Status Signal Processor is constructed of five blocks, as shown in Diagram 7-18, and basically functions as the emitter of the Focus/Tracking Servo and Tracking Search control and status signal.
TC9201BF operates the Focus/Tracking and Tracking Search with the four signals, FE, TE, SBAD and RFRP, input from TA8101N. The AD Convertion Block, as shown in Diagram 7-18, takes the four signals that are input after passing through the TA8101N internal comparator and passed through the TC9201BF internal 5-bit Up/Down Counter, 5-bit DA Converter, which make up a demodulation loop. This construction is thus a Follow-up Comparison Type 5-bit AD Conversion Circuit. This AD converted data is used for internal digital signal processing.

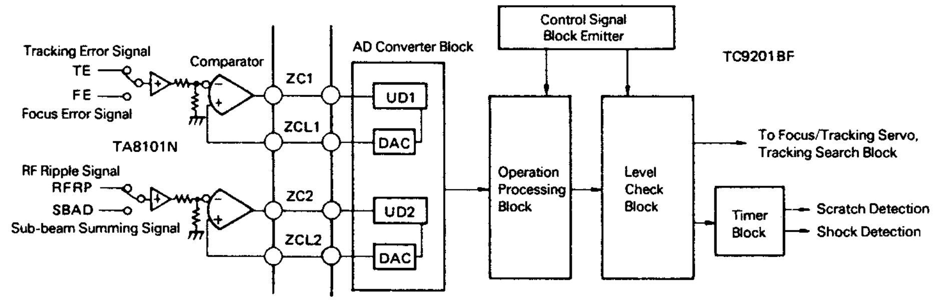


Diagram 7-18 Servo Status Signal Processor Block Construction

By using the TA8101N Comparator Output ZC1 and ZC2, the Up/Down Counter, UD1 and UD2, controls at about 500 kHz with $(10000)_2$ as the center is divided into 32 levels. Then a 0~VREF (+2.2 V) voltage range is emitted from the 5-bit DA Converter Output ZC1 and ZC2 (See Diagram 7-19)

The internal digital signals processed are not the actual data that has been AD converted but a four-sample average data. The reason for this is that, when using a Follow-up Comparison AD Converter, the Up/Down Counter is constantly moving back and forth between +1 and −1 which makes it difficult to use this data as it is. The converted data also includes noise, which needs to be taken out. This sampling method therefore takes out the high range noise content.
Also, the Operation Processing Block receives data through the two AD Converters and operation processes them in the ALU (Operation Unit) and thus emits the required signals for Focus/Tracking Control.

The data calculated in the Operation Processing Block is passed through the Level Check Block where this input data is continuously being detected. The aquired Detection Result is transferred to the Focus/Tracking Servo and Tracking Search Block.

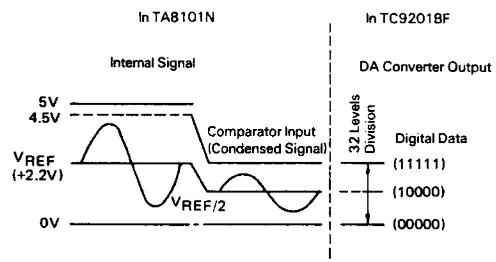


Diagram 7-19 Data Division Details during AD Conversion

CIRCUIT DESCRIPTION

2) Focus/Tracking Servo System

Focus/Tracking Servo and Tracking Search system operations are actually divided into modes, as shown in Chart 7-4. Operations are done with a 2 MHz System Lock with four clocks per mode.

SEL PIN OUTPUT	SYSTEM MODE DIVISION	MONITOR SIGNAL		OPERATION DETAILS
		UD1	UD2	
H	Focus Gain Adjustment Focus Search	FE	SBAD	Focus Gain Adjustment Focus Search, FOK (Focus ON) Detection
L	Tracking Gain Adjustment	TE	RFRP	Tracking Gain Adjustment RFRP Slice Level Calculations Output
HiZ	Non-Play Normal Play	TE	SBAD	Scratch and Shock Detection FOK (Focus ON) Detection
L	Special Play	TE	RFRP	Shock Detection RF Zero Cross Detection
L	Tracking Search	TE		Tracking Search

Chart 7-4 Focus/Tracking Servo Mode Division

Note #1: TC9201BF determines the information input from TA8101N with the SEL Output Signal
The four signals, FE (Focus Error), TE (Tracking Error), SBAD (Sub-beam Summing) and RFRP (RF Ripple) are divided into three by the SEL Output Signal.

Note #2: Non-Play is the condition in which eventhough the DMSV Command (CLV Servo ON) is set, Tracking is OFF (Detailed explanation excluded).

Note #3: Special Play is the condition after Tracking Search is complete and the next mode. Detailed explanation is done in the Tracking Search System.

The Focus/Tracking System is operated in accordance to the CPU Process Flow Chart on Page 79.
Starting with the Focus Gain System, the operation explanations of the systems in order are in the following.

DP-1510

CIRCUIT DESCRIPTION

(1) Focus Gain Adjustment (FGA) System

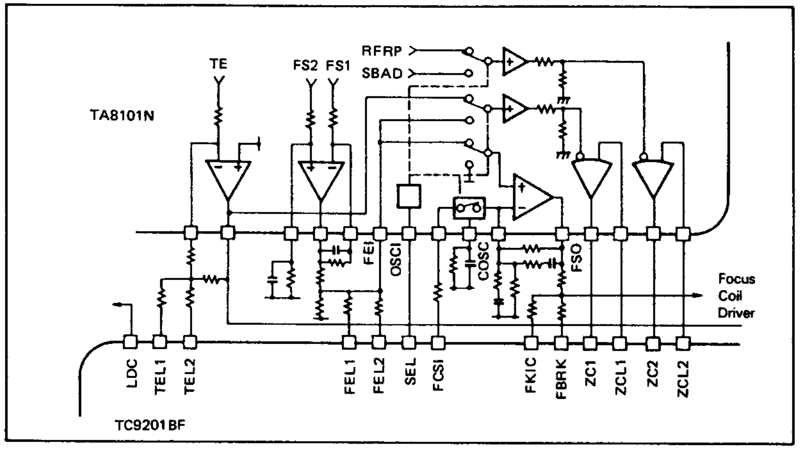


Diagram 7-20 System Construction Diagram

- Correlation Pins: FKIC, FEL1, FEL2, SEL
- Commands: FGASS(88xx), FGASR(89xx) FGASET(8Axx)
- Write Command (CM-A)
- Command Reception
  Conditions: LDON(84xx)
  Command Set

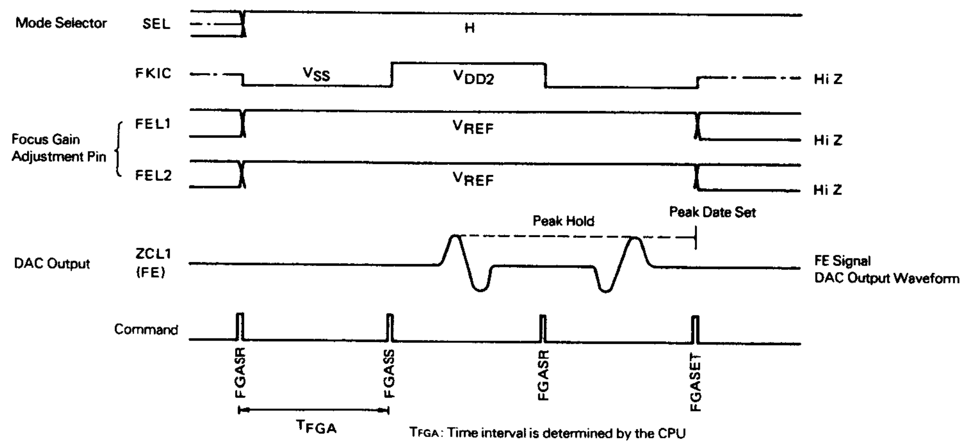


Diagram 7-21 Timing Chart (1)

CIRCUIT DESCRIPTION

By switching the two analog switches (FEL1 and 2) ON/OFF, the Focus Gain Adjustment System fixes the gain from the Focus Servo Open Loop and corrects the Pick-up and Disc dispersion. The three commands, FGASS, FGASR and FGASET are used here. The FGASS command is the electrical value of VDD2 from the FKIC pin and the FGASR command is the Vss electrical value. The Focus Actuator is moved vertically(moving the lense farther from and closer to the Disc). During the input of these commands, FEL1 and 2 forcefully made the VREF electrical value (with the least gain possible), and also the SEL pin becomes "H" level. When the SEL pin = "H", the Observation Signal from the Servo IC, TA8101N, is input in which the ZCL1 side is an FE signal and the ZCL2 side is the SBAD signal. Also, when FGASS and FGASR commands are input, ZCL1 side FE signal will go into Peak Data Hold Mode. The FGASET command determines the Peak Data Decoding Result to set FEL1 and 2. By using FEL1 and 2, the amplitude of FEI is adjusted to about 0.8 Vp-p. At this time the SEL pin will maintain an "H" level where the FKIC pin will maintain HiZ (operation completed) information. The intervals and number of times of FGASS and FGASR commands is set by the CPU and the FGSET command is output once.

BCD	Peak Data	FEL 1	FEL 2
10	10000	0	0
11	10001	0	0
12	10010	0	0
13	10011	0	0
14	10100	0	0
15	10101	0	0
16	10110	0	0
17	10111	1	0
18	11000	1	0
19	11001	0	1
1A	11010	0	1
1B	11011	1	1
1C	11100	1	1
1D	11101	1	1
1E	11110	1	1
1F	11111	1	1

0:FEL = HiZ 1:FEL = VREF

Chart 7-5 FE Signal Peak Data Code Chart

CIRCUIT DESCRIPTION

(2) Focus Search System

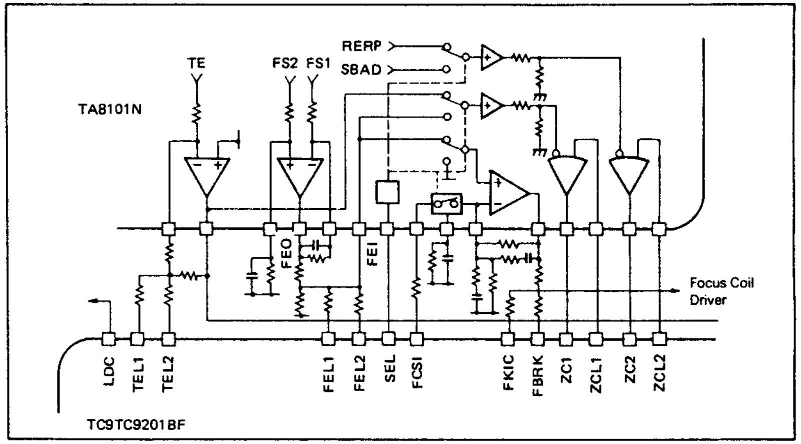


Diagram 7-22 System Construction Diagram

Correlation Pins: FCSI, FBRK, SEL
Commands: SDSET (80xx), FORST (8Fxx), STRD (1), FOSET (8Exx)
FOCUS (9AF$_1$ F$_2$)
F$_1$: FS Resistor Data
F$_2$: FCOK Resister Data
Command Reception Conditions: LDON(84xx) Command Set

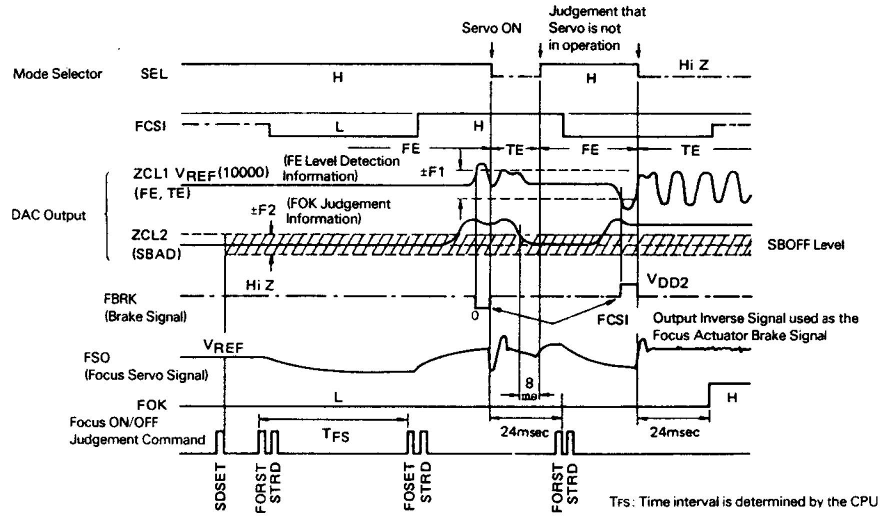


Diagram 7-21 Timing Chart (2)

CIRCUIT DESCRIPTION

The Focus Search System detects the cross over point of the laser beam from the Pick-up and the Disc and turns the Focus Servo ON at this point.

The following explains about Focus Search Operations (refer to Page 81. (c) CPU Process Flow Chart of Focus Search Method)

1 During Focus OFF (possible with the Laser Diode ON/OFF) the SBAD Data is read by the SDSET command to the internal resister. The Read Level is to be SBOFF.
2 Input the FOSET or FORST command and set the FOSI pin to "H" or "L" level.
3 With the FCSI Output Pin Level, the direction of current is designated to the Focus Coil, while at the same time the lense starts to move. The FE Signal of ZCL1 starts to change in accordance to the Timing Chart.
4 When the FE Signal surpasses the F1 Level, this means the Cross Over Point is near. Here the Focus Servo ON goes into Stand-by. At the same time, FBRK Signal goes from a HiZ condition to the opposite level signal output of the FCSI pin output. This FBRK is used as the Brake Signal and at the point of stabilization, the Focus Servo is turned ON.
5 Next the Zero Cross Point of the FE Signal is detected. This point is the Cross Over Point so the Servo is turned ON here. Also, FOK is selected after judging whether Focus has been achieved with the SBAD Signal Level.

The above was the Focus Search operations. The following are the internal judgement conditions as to whether Focus has been achieved or not.

Focus ON/OFF Judgement Conditions

Focus OFF → ON Judgement Conditions (Example: during POWER ON)

- $T_{NG} \geqq 8$ ms: Judged to be Focus OFF
  → FOK = H
  SEL pin: HiZ held
- $T_{OK} \geqq 24$ ms: Judged to be Focus ON
  → FOK = H
  SEL pin: HiZ held

Focus ON → OFF Judgement Conditions

- $T_{NG} \geqq 64$ ms: Judge to be Focus OFF
  FOK = H → L
  SEL pin: HiZ → "H" level

Note #1: T_{OK}: | SBAD − SBOFF | ≧ F2 level maintained period
(SBOFF is the SBAD data during SDSET command input)
T_{NG}: | SBAD-SBOFF | < F2 level period

Note #2: The system is designed to take the safe side in case of external disturbance in considering Focus ON → OFF or Focus OFF → ON conditions.

CIRCUIT DESCRIPTION

(3) Tracking Gain Adjustment (TGA) System

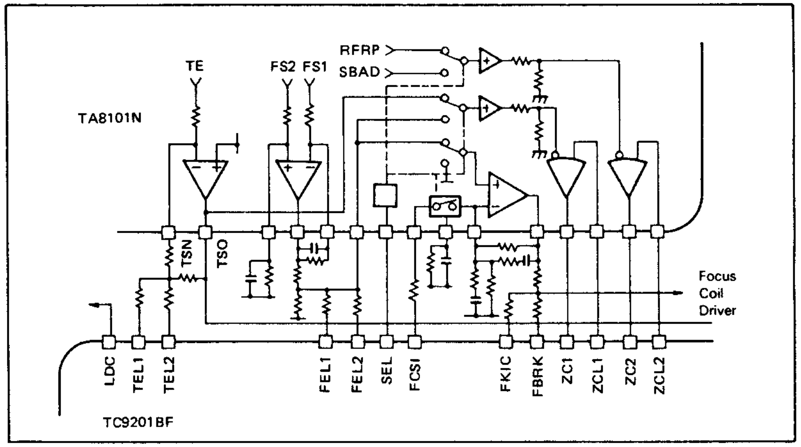


Diagram 7-24 System Construction Diagram

Correlation Pins: TKIC, TEL1, TEL2, SEL
Commands: TGASS (8Dxx), TGASR (8Cxx), TGASET (8Bxx)
Write Command (CM-A)
Command Reception Conditions: DMSV (86xx)
Command Set (FOK = To be H → Focus ON)

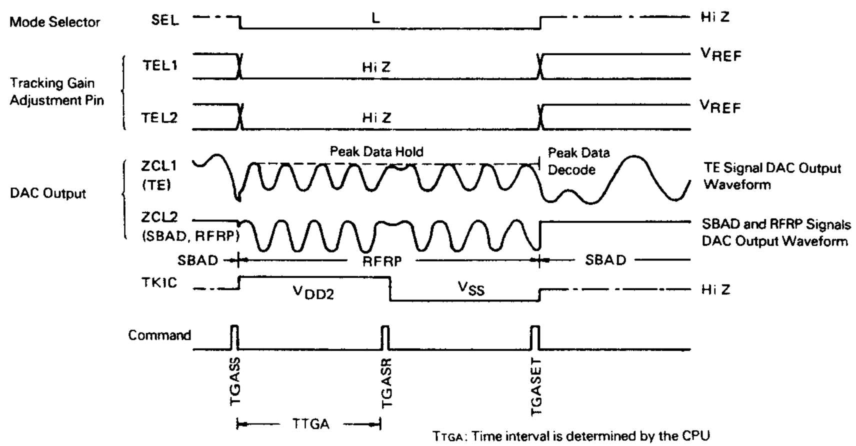


Diagram 7-25 Timing Chart (3)

By switching the two analog switches (TEL1 and 2) ON/OFF, by fixing the gain from the Tracking Servo Open Loop the Tracking Gain Adjustment System will take the Shock and Defect Detection Selectivity to be done equally (Tracking Error Signal Amplitude is fixed). Also to aquire the Zero Cross Timing of the RF Signal (needed information during Tracking Search) the Slice Level is calculated. The three command used are TGASS, TGASR and TGASET. The TGASS command is the electrical value of VDD2 from the FKIC pin and the TGASR command is the Vss electrical value. This means the Tracking Actuator is moved around internally and externally. During the input of these two commands, TEL1 and 2 are forcefully set to HiZ while the SEL pin is "L" level. When the SEL pin = "L", the Observation Signal from the Servo IC, TA8101N, is input in which the ZCL1 side is a TE signal and the ZCL2 side is the RFRP signal. When TGASS and TGASR commands are input, the TE signal of the ZCL1 side is put into Peak Data Hold Mode and when TGASET command is input, the Peak Data is decoded and set to TEL1 and 2. TEL1 and 2 go on to be used, as shown in the System Construction Diagram (Diagram 7-24), to adjust the TSO amplitude to about 0.8 Vp-p. The intervals and number of times of TGASS and TGASR commands is set by the CPU and the TGASET command is output once.

Note: When the Tracking Gain Adjustment System is run, it is taken for granted that the CLV Servo is in operation when the DMSV command is input.
The reason for this is that during Tracking Gain Adjustment, the RFRP signal is used to observe the Focus condition.

For further information about Tracking Search Operations, refer to Page 81, (d) CPU Process Flow Chart of Focus Search Method.

BCD	Peak Data	TEL 1	TEL 2
10	10000	1	1
11	10001	1	1
12	10010	1	1
13	10011	1	1
14	10100	1	1
15	10101	1	1
16	10110	0	1
17	10111	0	1
18	11000	1	0
19	11001	1	0
1A	11010	0	0
1B	11011	0	0
1C	11100	0	0
1D	11101	0	0
1E	11110	0	0
1F	11111	0	0

0:HiZ 1:VREF

Chart 7-6 TE Signal Peak Hold Data Decode Chart

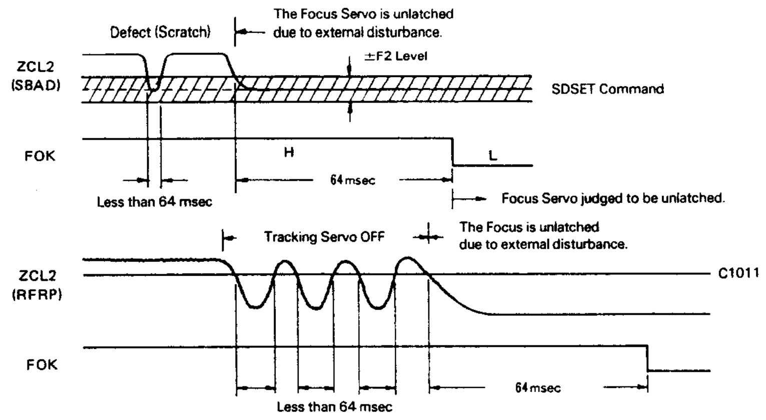


Diagram 7-26 SBAD and RFRP Signal Focus ON/OFF Comparison Signal

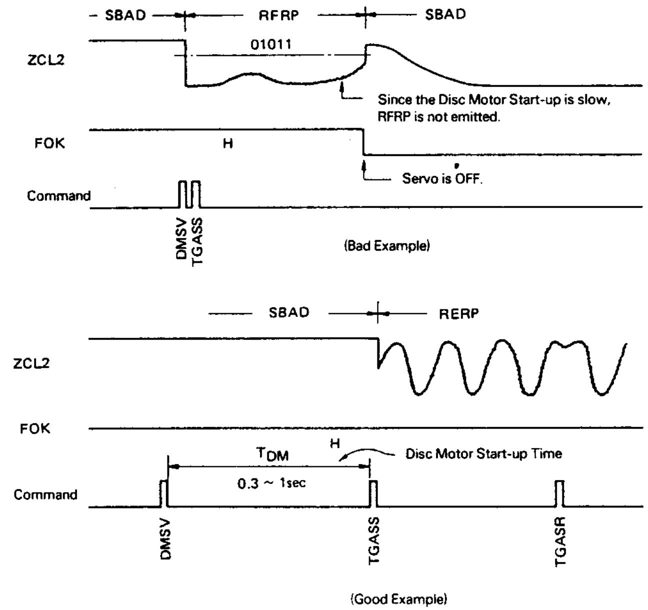


Diagram 7-27 RFRP Signal Output Waveform during Disc Motor Servo ON (DMSV Command Set)

(4) Tracking Search System

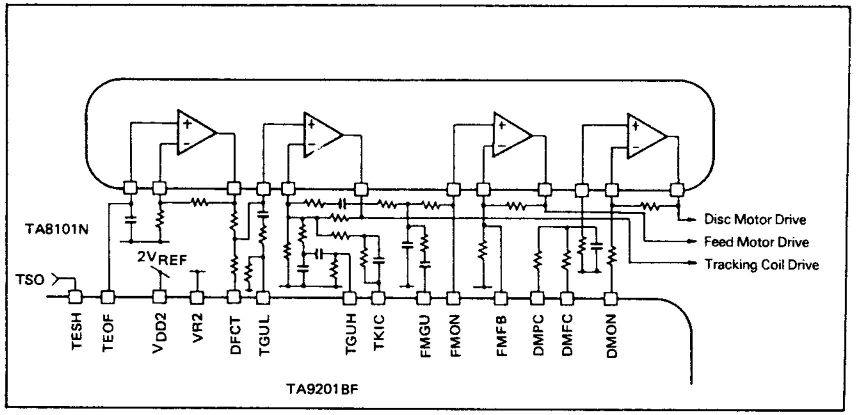


Diagram 7-28 System Construction Diagram

Correlation Pins: TESH, TEOF, TGUL, TGUH, TKIC, FMGU, FMON, FMFB, SEL

Commands: SETR2 (9F R_5 R_6) Write Command (CM-C)

PAUSE (ARs N_1)
FEED (BRs N_2)
NKIC (CRs N_1)
NKICF (DRs N_1)
CKIC (ERs T_0 N_3)
CKICF (FRs T_0 N_3)
STRD (1)
— Write Command (CM-D)

Command Reception Conditions: DMSV (86xx) Command Set (FOK is to = H → Focus ON)

Note: Each Command Bit Information

Data	R5	R6	Rs	T0
D3	GUP1	LDCP	BR	—
D2	HYS1	RFRG1	FGC	—
D1	GUP2	RFRG2	TGC	T
D0	HYS2	FMSS	B/F	T

N_1.........Number of Kick Track 8 bits N_1 Track Kick Amount (0 ~ 255)

N_2.........Number of Kick Track 8 bits 64 ×N2 Track Kick Amount (0 ~ 16320)

N_1.........Number of Kick Track 4 bits N1 Track Kick Amount (0 ~ 15)

T..........Kick Interval 2 bits during CKIC and CKICF (62 ms ~ 495 ms)

The basic operation of Tracking Search (after Search) are two types, Lense Kick Search (PAUSE, NKIC, NKICF) of the Pick-up and Pick-up Feed Motor Search (FEED). Beside this there is the Continuous Kick Search (CKIC, CKICF) of the Lease Kick that is done periodically.

The six types of search just mention are explained in the following.

1 PAUSE....With the Feed Motor Send OFF, 0 ~ 255 Track Lense Kick
After the Lense Kick operation is complete, the Feed Motor goes from STOP → PAUSE operation

2 FEED......Turn ON Feed Motor Send and Search. Send 64 × (0 ~ 255) Tracks

3 NKIC......With the Feed Motor Send OFF, 0 ~ 255 Track Lense Kick

4 NKICF.....Turn ON Feed Motor Send and NKIC Search.

5 CKIC......0 ~ 15 Track Lense Kick for fixed intervals.
→ Fast Forward, Fast Reverse operations

6 CKICF.....Turn ON Feed Motor Send and CKIC Search.

The Search System uses the count method of the number of tracks. Search commands such as, whether to apply the brake on the Track Lense Kick operation or not, whether the Search Direction should be Forward (FWD) or Backward (BWD), are selected in the 4 bit C3 ~ C0 of CM-D. For details, refer to Control Command (3) Write Command CM-D.

The basic Tracking Search Operations are shown in the Tracking Search Timing Chart, Examples 1 ~ 8, but for the Correlated Pin Operation, see the following.

- SEL Pin: As soons as search is complete, changes to "L" level, and switched to the TE and RFRP Signals input from TA8101N. As soon as this search is complete, returns level to HiZ. Only in the case that the bit data from HYS2 (see CM-C STR2 for details) in hysterisis operation, the "L" level is held for 2 ~ 3 ms after search completion.
- TSO Pin: During Forward Directional Search, the TE Signal becomes positive (+) polarity thus changing the Error Signal. During Backward Directional Search, the TE Signal becomes negative (−) polarity thus changing the Error Signal. } Be careful with polarity.
- ZCL1 Pin: During search this has a fixed output of VREF/2 (Digital Data = 10000).
- ZCL2 Pin: While= "L" level, the RFRP Signal is output.
- TKIC Pin: During PAUSE, NKIC, NKICF commands input:
  - (a) When in FWD Search, VDD2 output is fixed
  - (b) When in BWD Search, VSS output is fixed
  - (c) When BR bit data = 0 in (a) and (b), and when half the designated number of tracks, $N_1/2$ (When N_1 is an odd number, the Track OFF Point) is traversed, the TKIC pin becomes HiZ.
  - (d) When BR bit data = 1 in (a) and (b), and when half the designated number of tracks, $N_1/2$ (When N_1 is an odd number, the Track OFF Point) is traversed, the TKIC pin will output the opposite electrical value (Brake Pulse) and then change to HiZ after search is complete.

  During FEED command input:
  The TKIC pin is HiZ.
- TESH Pin: During Normal Play
  Is shorted with the TEOF pin and the Tracking Servo Signal is received from TA8101N.
  During Search
  The TESH pin is HiZ.
  During Special Play (2 ~ 3 ms period after completion of search)
  When the RFRP signal is smaller than the Slice Level, then HiZ. This means that this pin will have hysteresis characteristics.
- TEOF Pin: During Normal Play
  Is shorted with the TESH pin.
  During Search
  VREF fixed output.

- TGUL/H Pin: During Normal Play and Search
  - VREF fixed output. (Set to the lower gain side)
  - During Special Play
    - GUP2 bit data = 1 set → HiZ (Gain Up)
    - GUP2 bit data = 0 set → VREF fixed output.
- FMON Pin: During Normal Play ... HiZ
  - During NKIC and CKIC command input
    - FMSS bit data = 1 set → HiZ (The Lense Kick Signal is impressed on the Feed Motor.)
    - FMSS bit data = 0 set → VREF fixed output. (Feed Motor STOP)
  - During PAUSE command input
    - After the Lense Kick operation is complete the FMON pin is hold VREF (Feed motor stop) to next (CM-D) Search Command input.
  - During NKICF, CKICF and FEED Command input
    - VREF fixed output.
- FMFB Pin: During Normal Play ... HiZ
  - During NKICF, CKICF and FEED command input
    - (a) When in FWD Search . . . VDD2 is fixed.
    - (b) When in BWD Search . . . VSS is fixed.
    - (c) When BR bit data = 0 in (a) and (b) (No brake) and the designated number of tracks, N_1 is traversed, the FMFB pin becomes HiZ.
    - (d) When BR bit data = 1 in (a) and (b)(with brake) and the designated number of tracks, N_1 is traversed, the FMFB pin will output the opposite electrical value (Brake Pulse) and then change to HiZ after search is complete.
- FMGU Pin: See CM-D Write Command for details.

The above are the details for the Correlation Pins. When concidering the system the most important items will be the gain of the Tracking Servo AMP selection (TGUL/H pin correlation).

Also when using any of the Search Commands and operating the kick in FWD, the TKIC pin will be VDD2.

For this, the polarity signal of the TSO pin will have to be changed from "+" to match that of the Tracking Error Voltage.

DP-1510

CIRCUIT DESCRIPTION

(5) Normal Play Defect/Shock Detection System

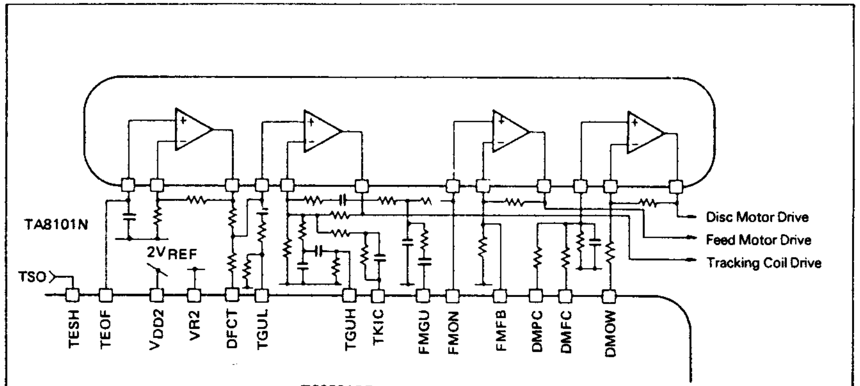


Diagram 7-29 System Construction Diagram

Correlation Pins: TESH, TGUL, TGUH, DFCT, FMGU, SEL

Commands: SETRO (98 R_1 R_2), SRCK (99 CK X), DEFECT-I (9B N TN), DEFECT-II (9CM TM), SHOCK (9 DL TL), SETR2 (9F R_5 R_6), NKIC (CRs 00), NKICF (DRs 00)

Command Reception Conditions: DMSV(84xx) Command Set (FOK is to be = H → Focus ON)

Note: Each Command Bit Information (for details see Write Command CM-C and CM-D.)

Data	R1	R2	R5	R6	Rs
D3	ATTC	MCG	GUP1	LDCP	BR
D2	MUTC	FSPS	HYS1	RFRG1	FGC
D1	$\overline{\text{HOSTP}}$	DIV+	GUP2	RFRG2	TGC
D0	GUPCL	DIV−	HYS2	FMSS	B/F

CK . . . . 4 bit data Tracking Error Signal and Through Rate Clock

N, M, L . . . . 4 bit data Defect/Shock Detection Sensitivity Level

TN, TM, TL . . . . 4 bit data Pulse Delay Timer for Defect/Shock Detection

CIRCUIT DESCRIPTION

In Normal Play, TC9201BF receives from TA8101N the TE Signal from the ZCL1 pin and the SBAD Signal from ZCL2 the pin. → AD Conversion.
With the input of the CM-D Search Command NKIC(00) or NKICF(00), Normal Play is put into operation. This is 0 Tracking Search.
At this time, the TE and SBAD Signals have already been Through Rate controlled. By comparing the data that has been Through Rate controlled and that that has been not, Defect Detection and CD Player System Shock Detection is executed.
The following explains about the defects, DFCT1 and DFCT2.

(a) DFCT1 → Black Dot at Read Out Side Defect Detection
(b) DFCT2 → Interuption in Information Layer Defect Detection

The following explains about Defect and Shock Detection operations.

I) DFCT1 Detection:
In the TE Signal of TC9201BF, when the absolute value of the difference between the TE and TESR (Through Rate Control) Signals surpasses N level (DEFECT-I Command Selection), the Defect Detection Signal, DFCT1, is emitted internally. The DFCT pin is then switched from HiZ to VREF (See Diagram 7-30).
At this time, the SRCK data is set by the SRCK command.
It is possible to adjust the Through Rate Clock in 15 stages (about 500 kHz × 0 ~ 15 CK). After the completion of Defect Detection, the Pulse Delay can be adjusted in 15 stages with about 0.062ms as one unit of T_N data.

II) DFCT2 Detection:
In the SB Signal, when the absolute value of the difference between the SB and SBSR (Through Rate Control) Signals surpasses M level (DEFECT-II Command Selection), the Defect Detection Signal .DFCT2, is emitted in the same way as DFCT1.
The DFCT pin is then switched from HiZ to VREF (See Diagram 7-30).
At this time, SRCK is about 2.1 kHz. After the completion of Defect Detection, the Pulse Delay can be adjusted in 15 stages with about 0.062ms as one unit of T_M data.

III) SHOCK Detection
In the TE Signal, when the TESR Signal surpasses the ±L level in reference to VREF (10000 reference level at +2.2 V), a "SHOCK" occurs, at the same time the Shock Detection Pulse is emitted.
In Shock Detection, it is possible to control whether to use the Detection Results or not by switching the GUP1 or HYS1 from 1 or 0 as shown in the Timing Charts in Diagrams 7-31 and 32.

- GUP1: When "1" during Shock Detection in Play, the Tracking Servo is gained up.
- HYS1: When "1" during Shock Detection in Play, the Tracking Signal will have hysterisis characteristics.
- GUPCL: When "1" at the same time a defect is detected, the shock detected is void (DFCT = DFCT1 + DFCT2)
  → Shock Detection Reset, Defect Detection Priority Operation

Make the final decision for the details of items I ~ III using the result of system consideration.
The same goes for the usage of the TGUL, TGUH and DFCT pins.

CIRCUIT DESCRIPTION

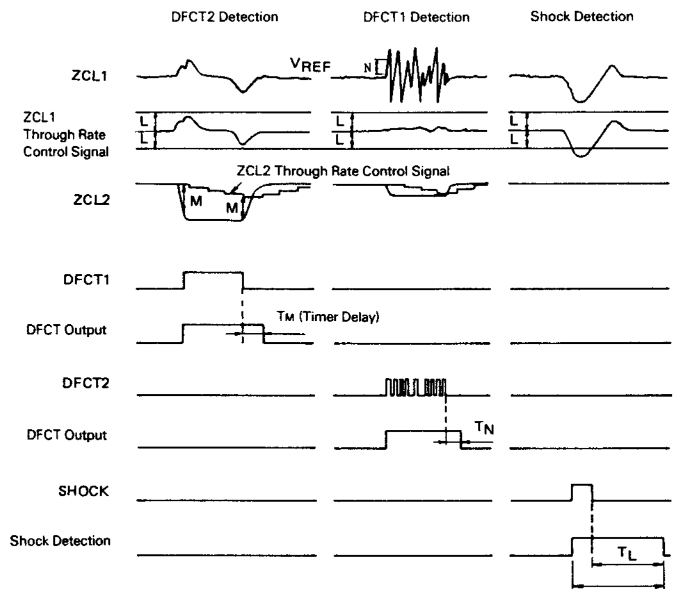


Diagram 7-30 Defect/Shock Detection

Data		Ck (kHz)	TN (msec)	TM (msec)	TL (msec)
Hexa-decimal	Binary				
0	0000	–	–	–	–
1	0001	260	0.060	0.060	0.97
2	0010	176	0.121	0.121	1.93
3	0011	132	0.181	0.181	2.90
4	0100	106	0.242	0.242	3.87
5	0101	88.2	0.302	0.302	4.84
6	0110	75.6	0.363	0.363	5.80
7	0111	66.2	0.423	0.423	6.77
8	1000	58.8	0.484	0.484	7.74
9	1001	52.9	0.544	0.544	8.71
A	1010	48.1	0.605	0.605	9.67
B	1011	44.1	0.665	0.665	10.64
C	1100	40.7	0.726	0.726	11.61
D	1101	37.8	0.786	0.786	12.58
E	1110	35.3	0.847	0.847	13.54
F	1111	33.1	0.907	0.907	14.51

Note: DEFECT-I and DEFECT-II data are set with the Shock Command

Chart 7-7 TN, TM, TL, Relation between Data and Setting Points

NKIC(C400) AND NKICF(D400) Search Command Set

GUP1 Bit Data = 1
HYS1 Bit Data = 0
FGC Bit Data = 1
TGC Bit Data = 0

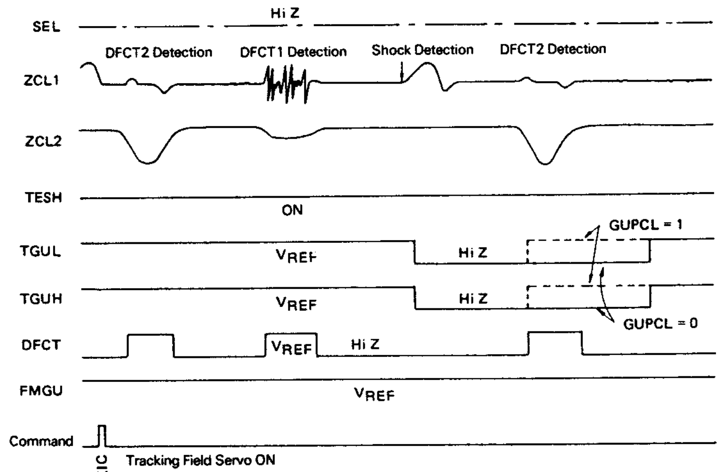


Diagram 7-31 Defect/Shock Detection Example 1

NKIC(C000) AND NKICF(D000) Search Command Set

GUP1 Bit Data = 0
HYS1 Bit Data = 1
FGC Bit Data = 0
TGC Bit Data = 0

Note: In Normal Play Mode, the SEL pin will become "L" level during hysterisis operation (HYS1 bit date = 1)

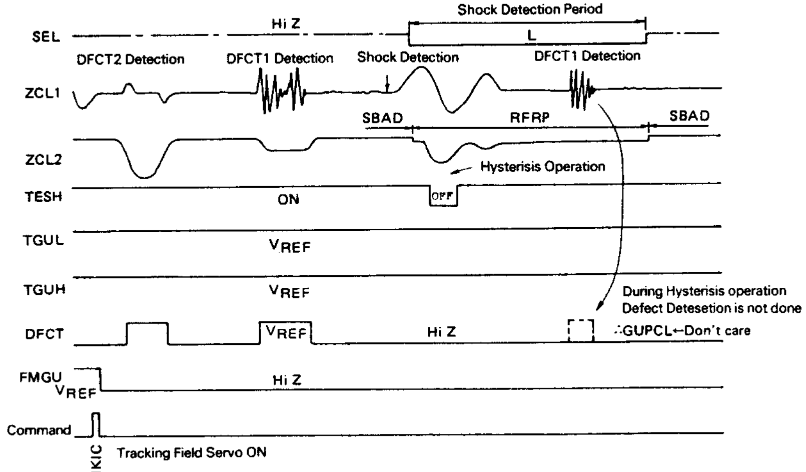


Diagram 7-32 Defect/Shock Detection Example 2

• Sub-code Q Receiving (RAM Control) Circuit

S0, S1, SUBQ, and SBOK Signals are transfered from TC9200BF.

In the Sub-code Q Data Receiving Circuit, the Sub-code Sychronizing Signal, S0 and S1, sychronize with the TC9201BF internal RAM Control Circuit to receive the 80 bit Sub-code Q Data into the internal RAM (4 bits × 20 words × 2 blocks).

The CPU checks the TC9201BF internal conditions and if Read Enable, the Read Command (STRD) is input. In response to this, TC9201BF sends the 4 bits with 20 words for a total of 80 bits to the CPU through BUS 3 ~ 0. The steps for this operation are explained in the following in reference to the N Block for Sub-code Q Data in the Timing Chart of Diagram 7-32.

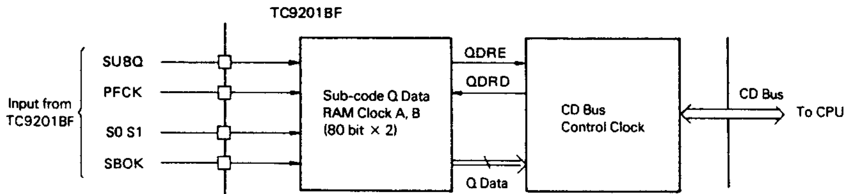


Diagram 7-33 Sub-code Q Data Receiving Circuit Construction

1 Synchronized to the RAM Control Circuit in the N Block S0 and S1.
2 The Sub-code Q Data that has been synchronized to the trailing edge of PECK (Play Mode 7.35 kHz), is output through the SUBQ pin in serial bit form of 96 bits (80 bits, data + 16 bits, CRCC). Of the 96 bits, only 80 bits are written into the internal RAM.
3 Confirm that SBOK is "H" level during (N+1) Block Data Input and set QDRE (Sub-Code Q Data Read Enable) Signal to "L" level (Read Enable). At this time, 4 bits (1 word) of Q data is preset to the internal resistor, and then the DA/CO line is switched to "L" level.
4 The CPU confirms whether Sub-code Q is in a Read Enable Condition. Confirmation is done by checking the DA/CO and BUS2 (QDRE Signal Monitor Line) lines in Idle Mode, and the input of the STRD Read Command in those not it Idle Mode and checking each BUS2 (QDRE Signal Monitor Line) lines.
5 If QDRE = "L" level then it is possible to read the Q Data into the CPU. The Read Command SQRD is input and 20 words (1 word = 4 bits) or 80 bits will be transfered to the CPU through BUS 3 ~ 0 with the timing shown in Diagram 7-35.

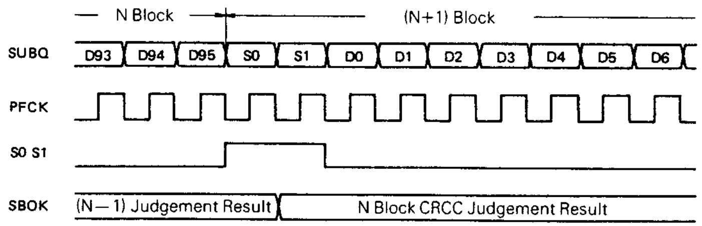
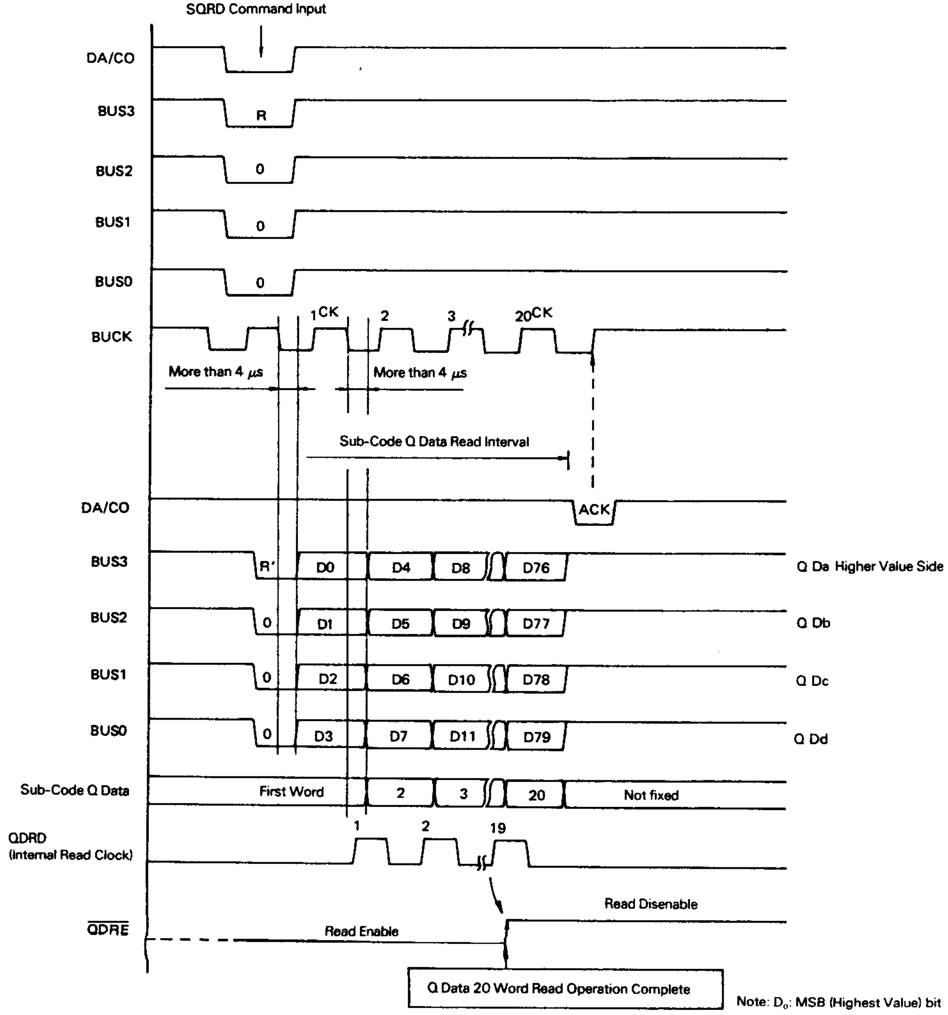


Diagram 7-34 Sub-code Q Data Reception Timing Chart

CIRCUIT DESCRIPTION

The above mentions were the steps in transfering of the Subcode Q Data to the CPU.
Also, the internal RAM divides the 80 bits into two blocks, A and B. This is to make it possible to write the Sub-code Q Data from TC9200BF and to read this to the CPU at the same time, individually. In other words, writing to A block while reading B block and visa versa is switched internally.
The QDRE Signal "L" level interval (Read Enable) is about 80 frames (about 10ms). Also when the SQRD command is input, 20 words of Q data are read while QDRE becomes "H" level. While Tracking Search is in operation, the QDRE Signal will not be set (to "L" level).



Note: D_0: MSB (Highest Value) bit

Diagram 7-35 Sub-code Q Data Read Process Timing Chart

CIRCUIT DESCRIPTION

- **Data Processor Interface Circuit**

1) Control Data (SCDA) Output Circuit

The information needed for internal processing in TC9200BF are serial output from the SCDA pin of TC9201BF. Each information is selected with the input of SETR0 and SETR1 commands, MUT ON/OFF and ATT ON/OFF commands from the CPU. Data output, in reference with the trailing edge of COFS, the Revison Mode Frame Synchronizing Signal,is continuously being transfered to TC9200BF.

Control Data Details

$\overline{ATT}$: −12 dB attenuation command ("L" for Attenuation ON)
Control is possible of the ATT ON/OFF with the SETR0 command (ATTC)

$\overline{MUTI}$: Forceful Muting Command ("L" for Muting ON)
Control of MUT ON/OFF is possible

MUTC: Internal Muting Control Command ("L" for Muting STOP)

$\overline{HOSTP}$: Correction Operation Stop Command ("L" for Correction Operation STOP)
Control of MUTC and HOSTP is possible with the SERT0 command.

ESGM, ESGL, WSEG: Control of the Selection Signal of the Frame Synchronizing Signal Compensation Circuit Correlation is possible with the SETR1 command.

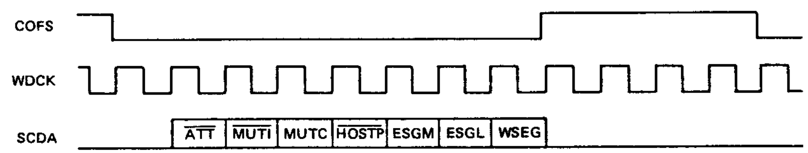


Diagram 7-36 Control Data Output Timing

2) Processer Status Data (SPDA) Input Circuit

Required information is serial input from the SPDA pin for the TC9200BF Status Data.
Each data input, in reference with the trailing edge of COFS, the Revison Mode Frame Synchronizing Signal, is continuously being transfered from TC9200BF.
Only three of the internal data of TC9201BF, FSPS, DIV+ and DIV− are used.

Processer Status Data Details

FSPS: Synchronized Status Flag ("L" for synchronized condition)

DIV+, DIV−: Disc Motor Control Signal

Note: For other data, see TC9200BF Technical Information of Page 40.

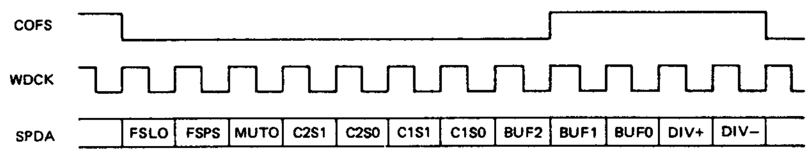
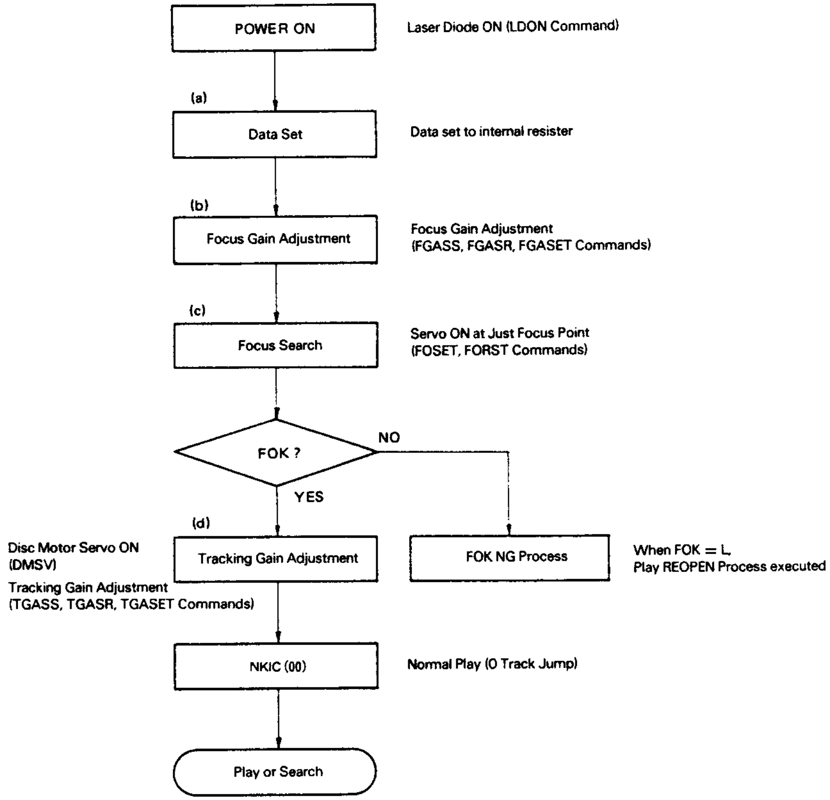


Diagram 7-37 Processer Status Data Input Timing

CIRCUIT DESCRIPTION

• CPU PROCESS FLOW CHART

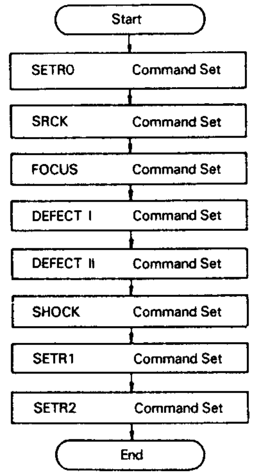
1) CPU Processing during POWER ON (Command Input Example)



For Data Set, Focus Gain Adjustment, Focus Search and Tracking Gain Methods details see (a) ~ (b).

CIRCUIT DESCRIPTION

(a) Data Set Method (internal resister set example)



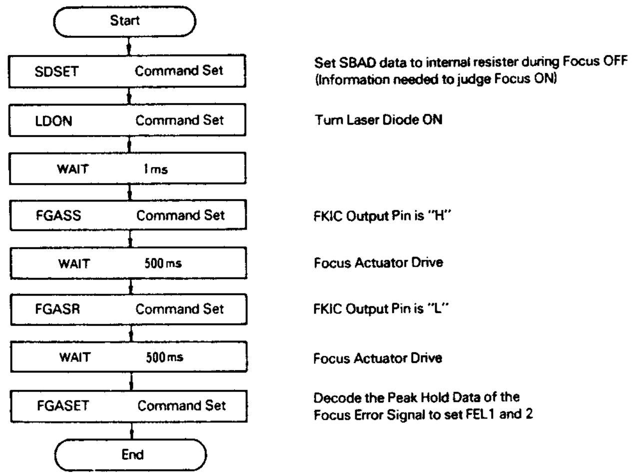
ATTC	MUTC	HOSTP	GUPCL	MCG	FSPS	DIV+	DIV−
1	1	1	0	0	0	0	0

SRCL Resister = 8 set
FS Resister = 5 set, FCOK Resister = 3 set
N Resister = 7 set, T_N Resister = 4 set
M Resister = 4 set, T_M Resister = 3 set
L Resister = 7 set, T_L Resister = 4 set

1	APCG 1	APCG 2	WSEG	ESGL	ESGM	1	DMG
1	0	0	1	1	0	1	0

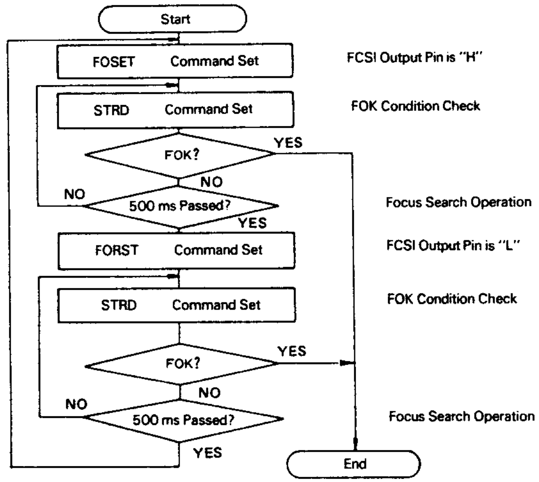
GUP 1	HYS 1	GUP 2	HYS 2	LDCP	RFRG 1	RFRG 2	FMSS
1	0	1	1	0	1	1	0

(b) Focus Gain Adjustment Method

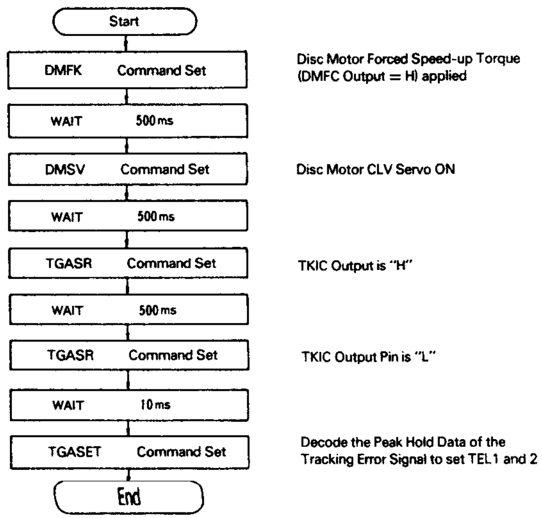


CIRCUIT DESCRIPTION

(c) Focus Search Method

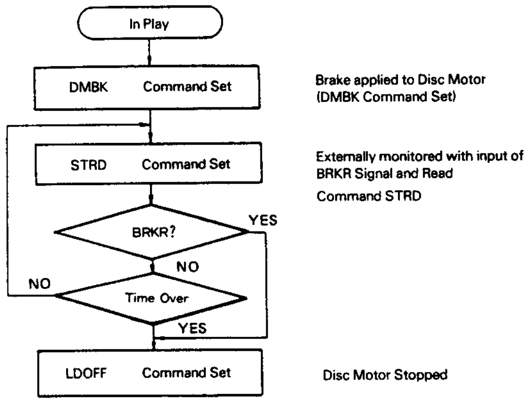


(d) Tracking Gain Adjustment Method



CIRCUIT DESCRIPTION

2) Stop Key Process

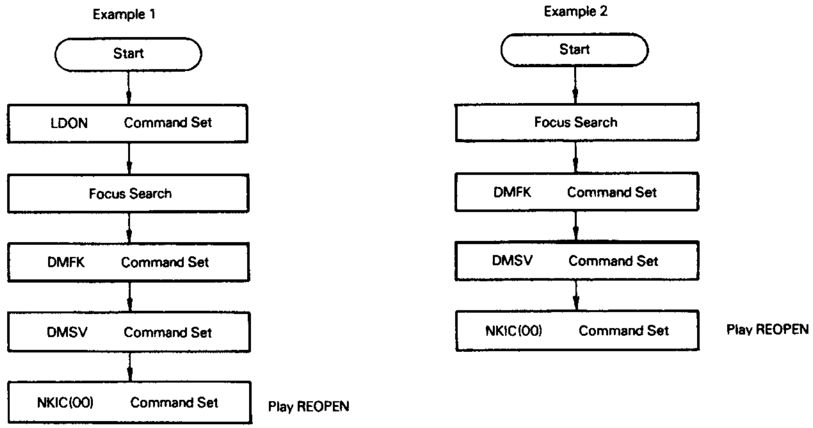


3) Processing for malfunctions

(Example 1) LD turned OFF with LD OFF Command. This command stops the Disc Motor.

(Example 2) When the FOK switches to "L" (Focus OFF Condition) in Play, the Disc Motor is stopped.

Play REOPEN Method

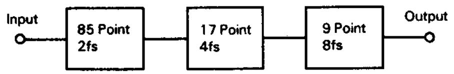


CIRCUIT DESCRIPTION

8. Digital Filter PD0036(X32-1400-10:IC10)

8-1. Functional Explanation

- Filter Construction



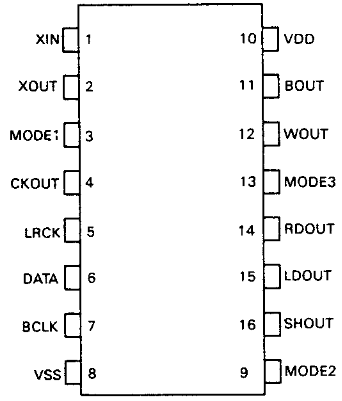
- Input Data
  Two complements, MSB First

- Output Data
  Two complements, MSB First

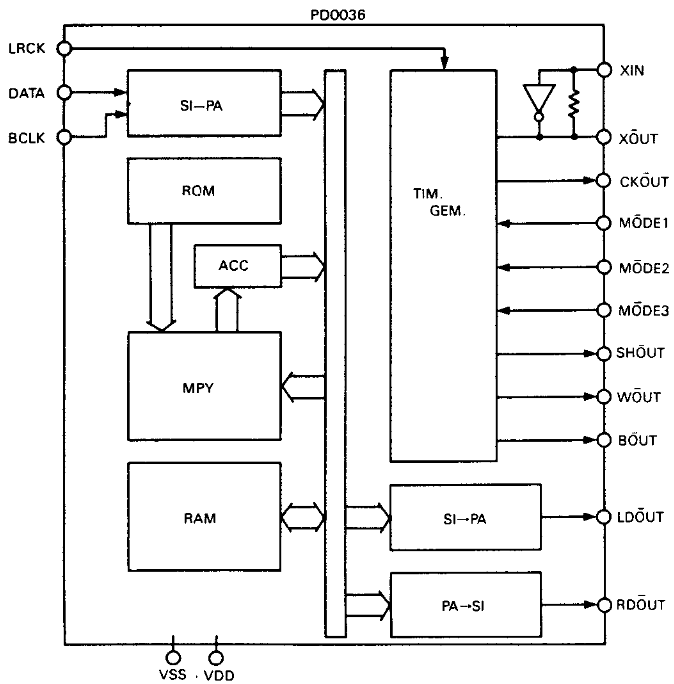
TTL Compatible

Jitter Free

8-2. PIN CONFIGURATION



8-3. BLOCK DIAGRAM



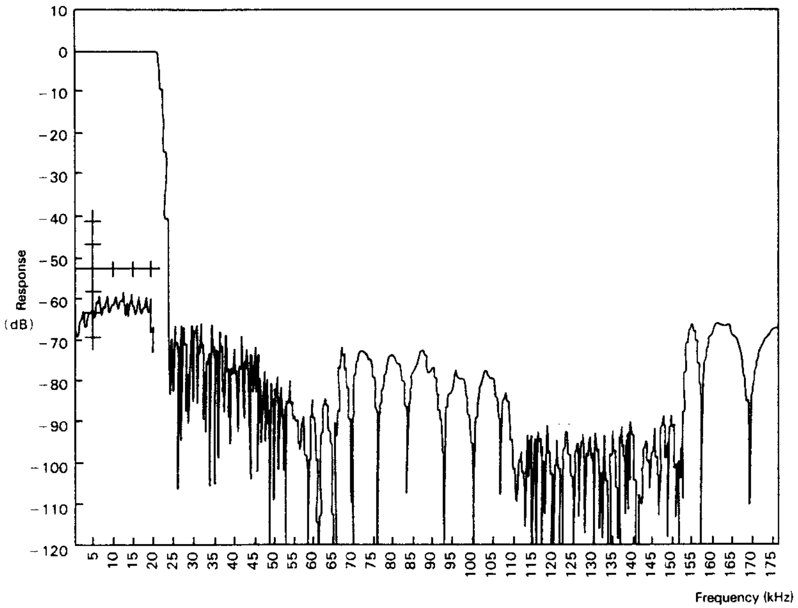
CIRCUIT DESCRIPTION

8-4. FILTER CHARACTERISTICS

Eight times Over Sampling Filter Frequency 0 ~ 176.4kHz

CHARACTERISTIC ITEM	PERFORMANCE
Pass Band	0 ~ 20 kHz
Stop Band	more than 24.1 kHz
Pass Band Ripple	within −0.02 ±0.01 dB
Stop Band Attenuation	more than 65 dB

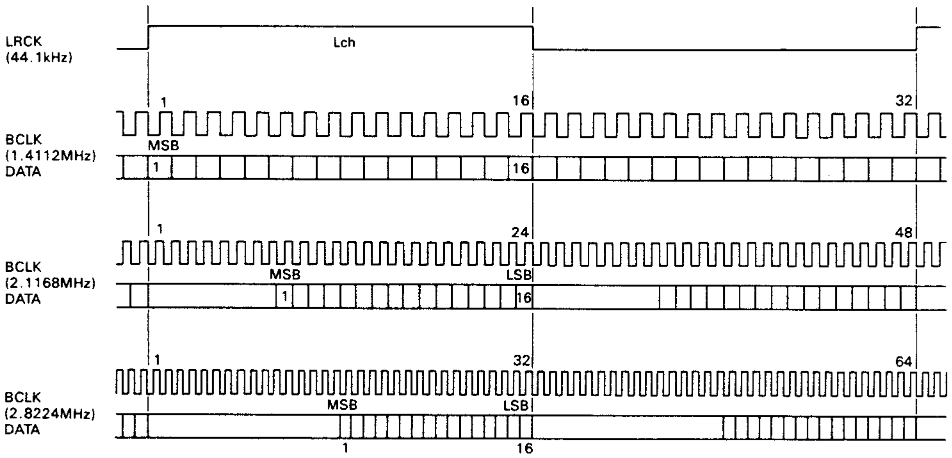
Sampling Frequency fs = 44.1 kHz



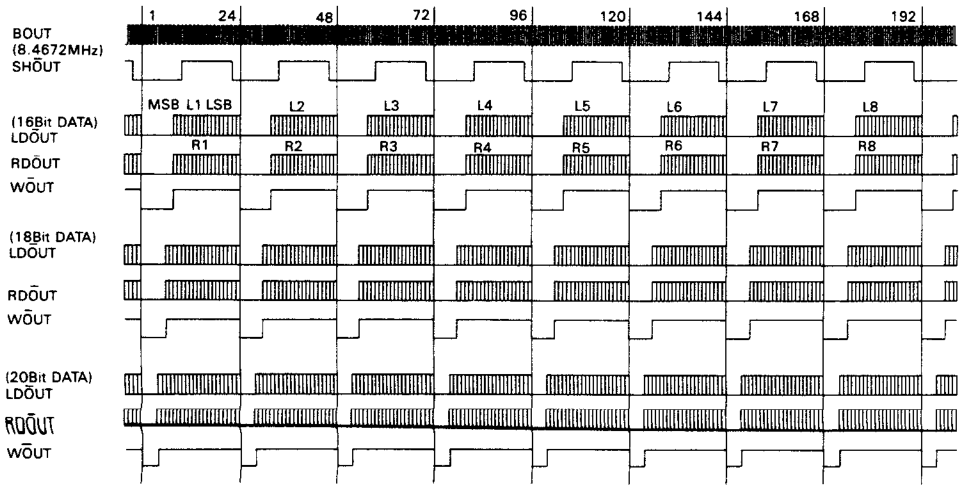
CIRCUIT DESCRIPTION

8-5. INPUT/OUTPUT TIMING

INPUT TIMING



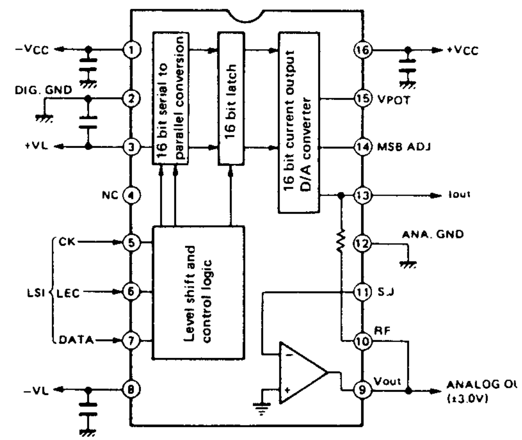
OUTPUT TIMING



CIRCUIT DESCRIPTION

9. D/A Converter PCM56P-L-1
(X32-1400-10: IC13, 14)

9-1. Pin Configuration and Block Diagram



9.2. Pin Configurations

Pin number	Pin name	Function
1	−Vcc	Analog Negative Power
2	DIG GND	Digital Ground
3	−VL	Logic Positive Power
4	NC	No Connection
5	CK	Clock Input
6	LED	Latch Enable Control Input
7	DATA	Data Input
8	−VL	Logic Negative Power
9	VOUT	Voltage Output
10	RF	Feedback Resister
11	S.J	Summing Junction (OP AMP input)
12	AND GND	Analog Ground
13	IOUT	Current Output
14	MSB ADJ	MSB Adjustment
15	V POT	Potentiometer
16	+Vcc	Analog Positive Power

MECHANISM DESCRIPTION
JAPAN MADE

MECHANISM OPERATION EXPLANATION

Diagram 1 shows the Mechanism Positions in STOP condition.
The following will explain the OPEN/CLOSE operations during Disc Loading and Vertical operation of the Pick-up Chasis.

Note #1) **In the operation explanation OPEN and CLOSE movement are shown as white and black arrows. See the following:**
Black Arrow: Tray will open in this direction (Tray OPEN)
White Arrow: Tray will close in this direction (Tray CLOSE)

Note #2) **The numbers in the parenthesis after the part names in the following are the reference numbers in the Service Manual.**

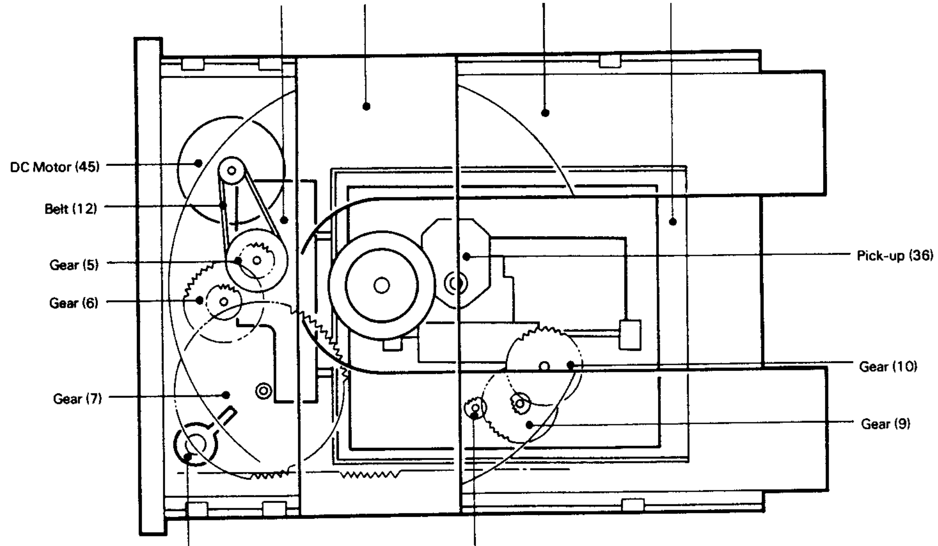


Diagram 1 Tray CLOSE Position

MECHANISM DESCRIPTION
JAPAN MADE

1. OPEN/CLOSE Operation of Tray

The DC Motor (❶) turns the gear (❷) that moves the tray in OPEN/CLOSE (❸).
OPEN/CLOSE is stopped when the latch on the gear turns the rotary switch (❹).

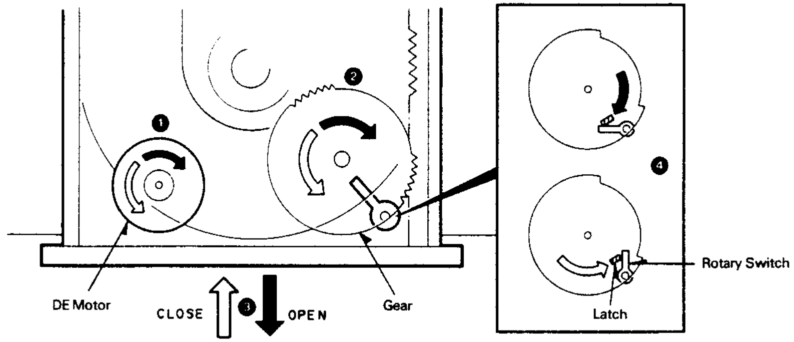


Diagram 2 Tray OPEN/CLOSE Operations

2. Vertical Movement of the Pick-up Chasis

Moving together with OPEN/CLOSE, the gear (❶) turn to move the slider (❷). The slide thus moves the Pick-up Chasis in the slots as shown in (❸).

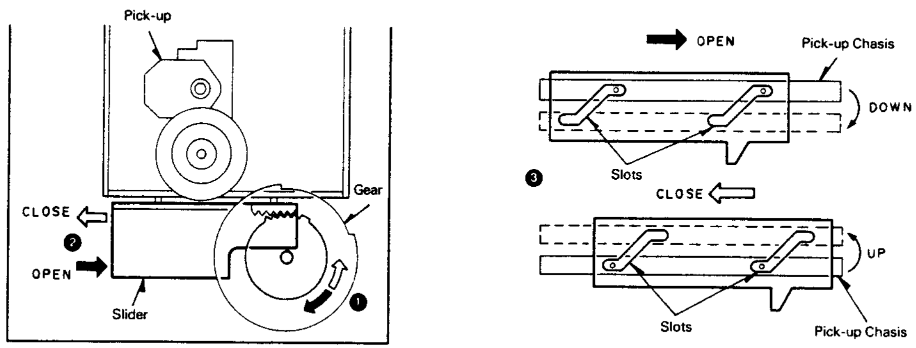


Diagram 3 Pick-up chassis UP/DOWN movement

MECHANISM DESCRIPTION
JAPAN MADE

3. Gear Setting Position
With the Pick-up Chasis is the lower position, set the gear to the position shown in (A).

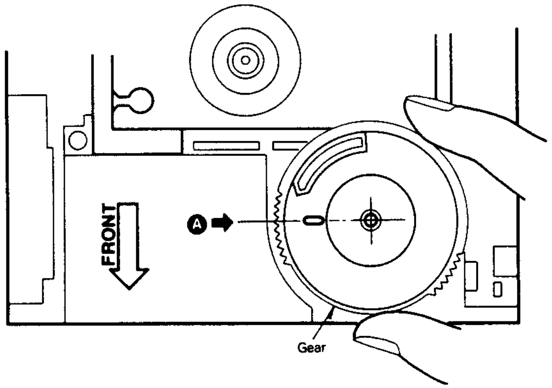


Diagram 4 Gear Setting Position

MECHANISM DESCRIPTION
SINGAPORE MADE

Mechanism Operation Description
Fig. 1 shows the relationship of mechanisms in the STOP mode. The OPEN/CLOSE operation of the mechanism and the UP/DOWN operation of the pickup chassis when loading the disc are described below.

Note 1 : The black arrow (OPEN) and the white arrow (CLOSE) in the operation description have the following meanings :

Black arrow (OPEN) : Tray opening direction (Tray OPEN)

White arrow (CLOSE) : Tray closing direction (Tray CLOSE)

Note 2 : Figures in the bracket ( ) in the operation description or accompanied with the part name in the diagram show the reference numbers in the Exploded View.

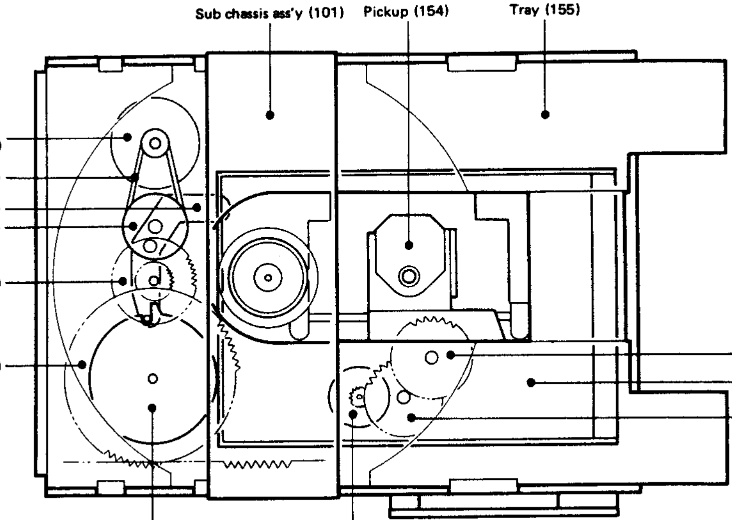


Fig. 1 Tray closed status

MECHANISM DESCRIPTION SINGAPORE MADE

SINGAPORE MADE

1. Tray OPEN/CLOSE Operation

By the rotation of the DC motor (1), the drive gear (2) is rotated to provide the tray OPEN/CLOSE operation (3).

The tray OPEN/CLOSE operation stops when the protrusion of the drive gear comes into contact with the leaf switch (4).

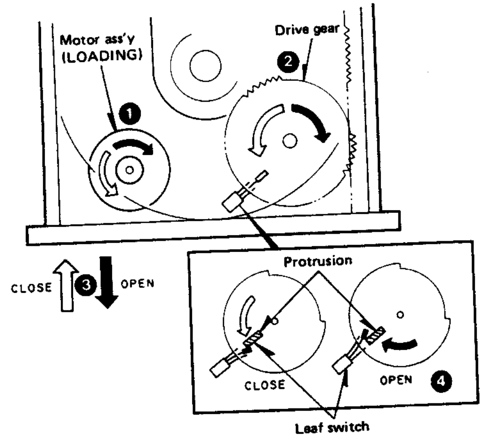


Fig. 2 Tray OPEN/CLOSE operation

2. Pickup Chassis UP/DOWN Movement

The control cam attached coaxially with the drive gear rotates in response to the tray OPEN/CLOSE operation (5). By this rotation, the protrusion of the pickup chassis moves along the groove of the control cam (6) so that the pickup chassis moves UP and DOWN correspondingly(7).

When the pickup chassis ascends fully by the rotation of the control cam in the UP (CLOSE) direction (8), the pickup chassis is locked by the lever (9).

When the control cam rotates in the DOWN (OPEN) direction (10), the pickup chassis is unlocked (11).

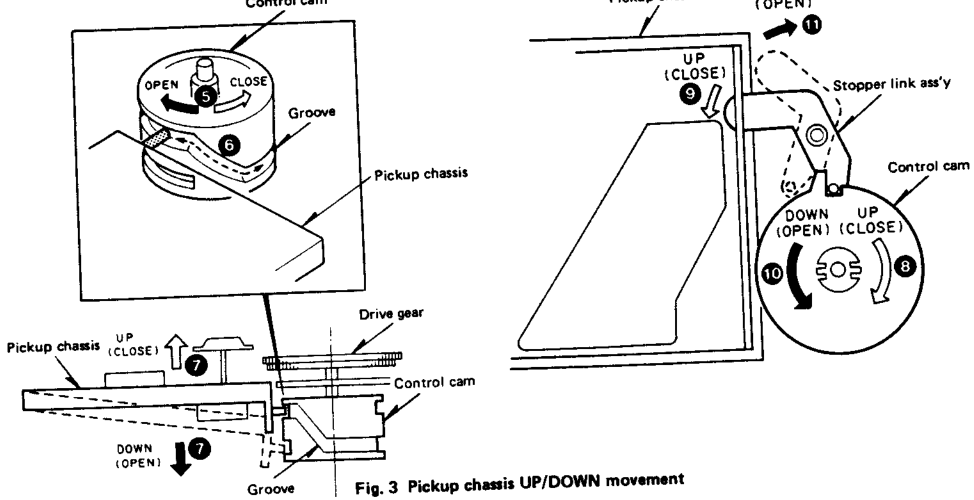


Fig. 3 Pickup chassis UP/DOWN movement

ADJUSTMENT

No.	ITEM	INPUT SETTINGS	OUTPUT SETTINGS	PLAYER SETTING	ALIGNMENT POINTS	ADJUSTMENT METHOD	DIA-GRAM
1	Laser Power	–	Place the sensor of the Light Power Meter on the Pick-up Lense	POWER ON while shorting the Test pin to put into Test Mode. Press the Manual S. Key ▶▶ to move the Pick-up to the periphery. Press the CHECK key to confirm the LD is in operation. Confirm that 03 is displayed.	–	With the power of 0.1 ~ 0.3 mV, the Pick-up is "OK" if the RF level is more than 1.0 Vp-p and TE (Servo OPEN) is more than 0.5 Vp-p in the correct diffraction grid.	(a)
2	Tracking Coil DC Offset	–	Connect a DC Voltmeter or an Oscilloscope to both pins of CN6.	Press STOP key. Confirm that the display shows 01.	TRACKING COIL DC OFFSET VR6 (X32-1400)	0±10 mV	(b)
3	Tracking Error Balance	TEST DISC TYPE 4	Connect an oscilloscope to CH1:RF (X32-1400:CN2-1) and CH2:TE (X32-1400:CN3-3). Note that the GND of the oscilloscope is to be connected to CN3-1 (VREF).	Press REPEAT and OPEN Tray. Set Disc and push tray in to CLOSE by hand. Press CHECK key and confirm that the display reads 03.	TE·BALANCE VR1 (X32-1400)	Vertically Symmetrical or DC = 0 ±0.05 V	(c)
4	Focus Error Balance	TEST DISC TYPE 4	Connect an oscilloscope to CH1:RF (X32-1400:CN2-1) and CH2:TE (X32-1400:CN3-3). Note that the GND of the oscilloscope is to be connected to CN3-1 (VREF).	Press PLAY key and confirm that 05 is displayed.	FE·BALANCE VR4 (X32-1400)	Best Eye Pattern	(d)
5	Focus Gain	TEST DISC TYPE 4 Pass a 1.4 kHz 0.5 Vrms signal through Pin 2 of CN4(X32-1400)	Connect a LPF to Pin 1 of CN4. Connect this to an oscilloscope or an AC Voltmeter (X32-1400).	Press PLAY key and confirm that 05 is displayed.	FOCUS GAIN VR3 (X32-1400)	50 mVrms	(e)
6	Tracking Gain	TEST DISC TYPE 4 Pass a 1.4 kHz 0.5 Vrms signal through Pin 2 of CN4 (X32-1400).	Connect a LPF to Pin 5 of CN4. Connect this to an oscilloscope or an AC Voltmeter (X32-1400).	Press PLAY key and confirm that 05 is displayed.	TRACKING GAIN VR2 (X32-1400)	50 mVrms	(e)

Note: Type 4 Disc — SONY·YEDS-18 Test Disc or the equivalent.

REGLAGE

N°	SUJET	REGLAGES D'ENTREE	REGLAGES DE SORTIE	REGLAGE DU LECTEUR	POINTS D'ALIGNEMENT	METHODE D'AJUSTEMENT	DIA-GRAMME
1	Puissance laser	—	Placer le détecteur du compteur de puissance lumineuse sur la lentille du capteur.	Fournir l'alimentation tout en court-circuitant la broche test pour entrer en mode test. Presser la touche Manual S. ▶▶ pour déplacer le capteur jusqu'à la périphérie. Presser la touche CHECK pour s'assurer que LD fonctionne. S'assurer que 03 est affiché.	—	Avec la puissance 0,1—0,3 mV, le capteur est bon si le niveau HF est supérieur à 1,0 Vc-c et TE (servo ouvert) est supérieur à 0,5 Vc-c dans le réseau de diffraction correct.	(a)
2	Décalage CC de bobine d'alignement	—	Raccorder un voltmètre CC ou un oscilloscope aux deux broches de CN6.	Presser la touche STOP. S'assurer que l'affichage indique 01.	VR6 DE DECALAGE CC DE BOBINE D'ALIGNEMENT (X32-1400)	0 ± 10 mV	(b)
3	Balance d'erreur d'alignement	DISQUE TEST DE TYPE 4	Raccorder un oscilloscope à CH1: RF (X32-1400: CN2-1) et CH2: TE (X32-1400: CN3-3). Remarquer que GND de l'oscilloscope doit être raccordé à CN3-1 (VREF).	Presser REPEAT et ouvrir le tiroir. Placer le disque et pousser le tiroir à la main pour le fermer. Presser la touche CHECK et s'assurer que l'affichage indique 03.	VR1 de TE-BALANCE (X32-1400)	Symétrique verticalement ou CC=0±0,05 V	(c)
4	Balance d'erreur de mise au point	DISQUE TEST DE TYPE 4	Raccorder un oscilloscope à CH1: RF (X32-1400: CN2-1) et CH2: TE (X32-1400: CN3-3). Remarquer que GND de l'oscilloscope doit être raccordé à CN3-1 (VREF).	Presser la touche PLAY et s'assurer que 05 est affiché.	VR4 de FE-BALANCE (X32-1400)	Meilleure forme	(d)
5	Gain de mise au point	DISQUE TEST DE TYPE 4 Passer un signal de 1,4 kHz 0,5 Vrms par la broche 2 de CN4 (X32-1400)	Raccorder un FPB à la broche 1 de CN4. Raccorder ceci à un oscilloscope ou à un voltmètre CA (X32-1400)	Presser la touche PLAY et s'assurer que 05 est affiché.	VR3 de GAIN DE MISE AU POINT (X32-1400)	50 mVrms	(e)
6	Gain d'alignement	DISQUE TEST DE TYPE 4 Passer un signal de 1,4 kHz 0.5 Vrms par la broche 2 de CN4 (X32-1400)	Raccorder un FPB à la broche 5 de CN4. Raccorder ceci à un oscilloscope ou à un voltmètre CA (X32-1400)	Presser la touche PLAY et s'assurer que 05 est affiché.	VR2 de GAIN D'ALIGNEMENT (X32-1400)	50 mVrms	(e)

Remarque: Disque de type 4 — Disque test SONY YEDS-18 ou équivalent.

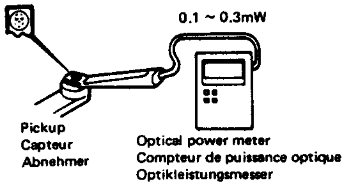
ABGLEICH

Nr.	GEGENSTAND	EINGANGS-EINSTELLUNGEN	AUSGANGS-EINSTELLUNGEN	SPIELER-EINSTELLUNG	ABGLEICH-PUNKTE	EINSTELLMETHODE	DIA-GRAMM
1	Laser-Leistung	—	Den Sensor des Lichtleistungsmeters auf die Abtasterlinse setzen.	Die Spannungs-versorgung einschalten, während der Teststift kurzgeschlossen wird, um den Testmodus zu aktivieren. Die Taste Manual S. (▶▶) drücken, um den Abtaster nach außen zu bewegen. Die CHECK-Taste drücken, um sicherzustellen, daß der LD in Betrieb ist. Sicherstellen, daß 03 angezeigt wird.	—	Bei einer Leistung von 0,1 — 0,3 mV ist der Abtaster in Ordnung, wenn der HF-Pegel mehr als 1,0 Vs-s und TE (Servo offen) mehr als 0,5 Vs-s im richtigen Beugungsgitter beträgt.	(a)
2	Spurhaltespulen-Gleichstrom-Versatz	—	Ein Gleichstrom-Voltmeter oder ein Oszilloskop an beide Stifte von CN6 anschließen.	Die STOP-Taste drücken. Sicherstellen, daß 01 angezeigt wird.	SPURHALTE-SPULEN-GLEICHSTROM-VERSATZ VR6 (X32-1400)	0 ± 10 mV	(b)
3	Spurhaltefehler-Balance	TESTDISC TYP 4	Ein Oszilloskop an CH1: RF (X32-1400: CN2-1) und CH2: TE (X32-1400: CN3-3) anschließen. GND des Oszilloskops muß an CN3-1 (V_{REF}) angeschlossen werden.	REPEAT drücken und Discträger öffnen. Die Disc einsetzen und den Discträger mit der Hand schließen. Die CHECK-Taste drücken und sicherstellen, daß 03 angezeigt wird.	TE-BALANCE VR1 (X32-1400)	Vertikal symmetrisch oder Gleichstrom = 0 ± 0,05 V	(c)
4	Fokusfehler-Balance	TESTDISC TYP 4	Ein Oszilloskop an CH1: RF (X32-1400: CN2-1) und CH2: TE (X32-1400: CN3-3) anschließen. GND des Oszilloskops muß an CN3-1 (V_{REF}) angeschlossen werden.	Die PLAY-Taste drücken und sicherstellen, daß 05 angezeigt wird.	FE-BALANCE VR4 (X32-1400)	bestes Augenmuster	(d)
5	Fokus-verstärkung	TESTDISK TYP 4 Ein Signal von 1,4 kHz, 0,5 Vrms durch Stift 2 von CN4 (X32-1400) senden.	Ein TPF an Stift 1 von CN4 anschließen. Dieses mit einem Oszilloskop oder Wechselstrom-Voltmeter verbinden (X32-1400).	Die PLAY-Taste drücken und sicherstellen, daß 05 angezeigt wird.	FOKUS-VERSTÄRKUNG VR3 (X32-1400)	50 mVrms	(e)
6	Spurhalte-verstärkung	TESTDISC TYP 4 Ein Signal von 1,4 kHz, 0.5 Vrms durch Stift 2 von CN4 (X32-1400) senden.	Ein TPF an Stift 5 von CN4 anschließen. Dieses mit einem Oszilloskop oder Wechselstrom-Voltmeter verbinden (X32-1400).	Die PLAT-Taste drücken und sicherstellen, daß 05 angezeigt wird.	SPURHALTE-VERSTÄRKUNG VR2 (X32-1400)	50 mVrms	(e)

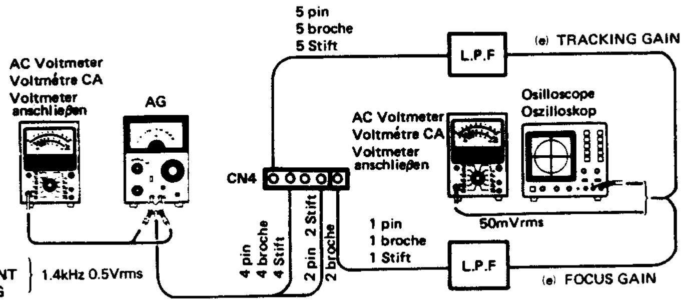
Hinweis: Testdisc Typ 4 — SONY Testdisc YEDS-18 oder äquivalent.

ADJUSTMENT/REGLAGE/ABGLEICH

(a) Laser Power



(e) Focus Gain, Tracking Gain



FOCUS GAIN
GAIN DE MISE AU POINT
FOKUSVERSTÄRKUNG } 1.4kHz 0.5Vrms

TRACKING GAIN
GAIN D' ALIGNMENT
SPURHALTEVERSTÄRKUNG } 1.4kHz 0.5Vrms

DP-1510

ADJUSTMENT

(a) Diffraction Grid Confirmation

(Picture 1) (20msec/div)

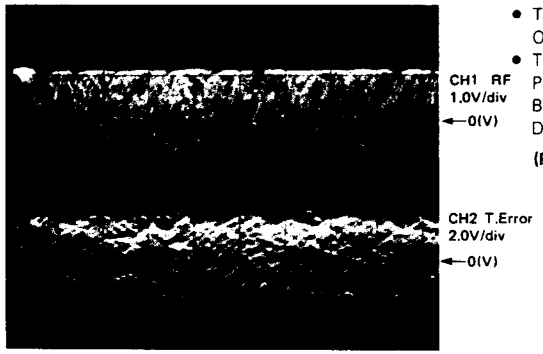
- RF and T. Error Signals when Diffraction Grid is correct.
(Picture 1)

(Picture 2) (20msec/div)

Trigger Point

- RF and T. Error Signals when Diffraction Grid is slightly OFF.
- The T. Error is small, and the envelope is as shown below.

(Picture 2)

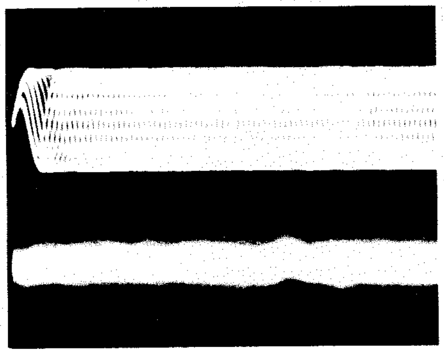


(Picture 3) (2μsec/div) Bump

- The RF and T. Error Signals during Test Mode (Focus ON)
- There is a "bump" in the T. Error when the RF Trigger Point is shown in the picture when the Sub- and Main Beams are in the same bit on a track in tracing during Diffraction Grid Adjustment.

(Picture 3)

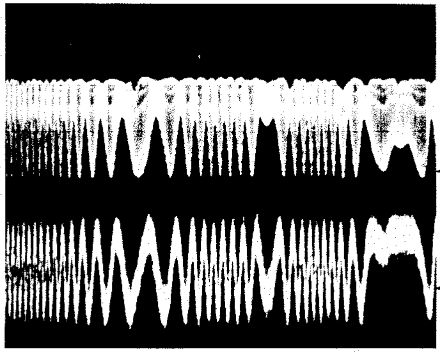
ADJUSTMENT



(Picture 4) (2μsec/div)

- The RF and E. Spot Signals during Test Mode (Play).
- When the Diffraction Grid is correctly adjusted, the E. Spot trigger (bump) can be confirmed about 12 μsec after the RF Signal. **(Picture 4)**

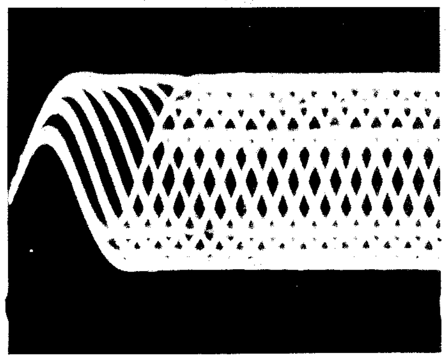
(c) Tracking Error Balance Adjustment



(Picture 5) (20msec/div)

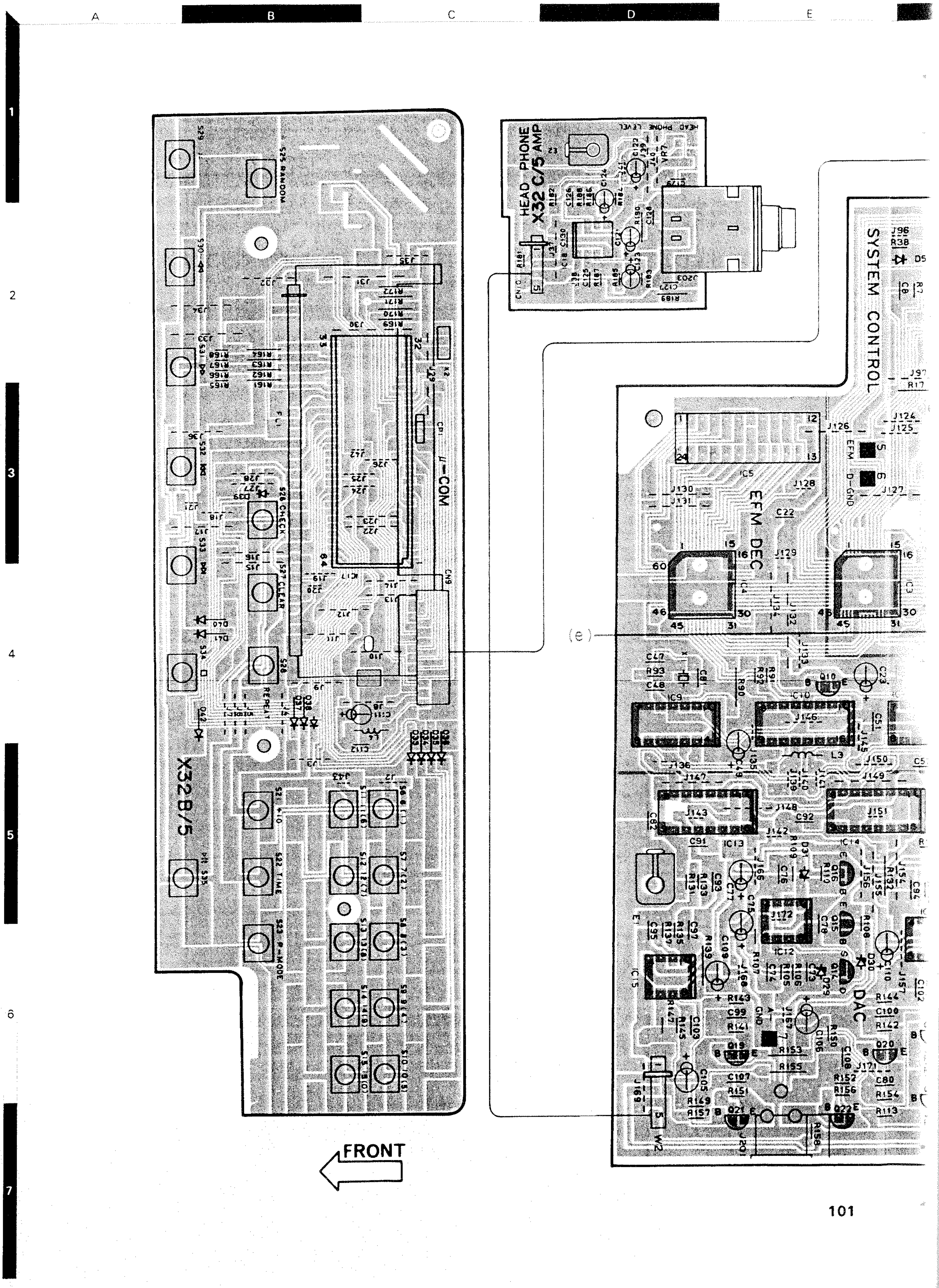
- The RF and T. Error Signals during Test Mode (Focus ON) (Test Disc Type: 4)
- T. Error is adjusted so that the symmetry is centered at 0 V (Tracking Balance). **(Picture 5)**

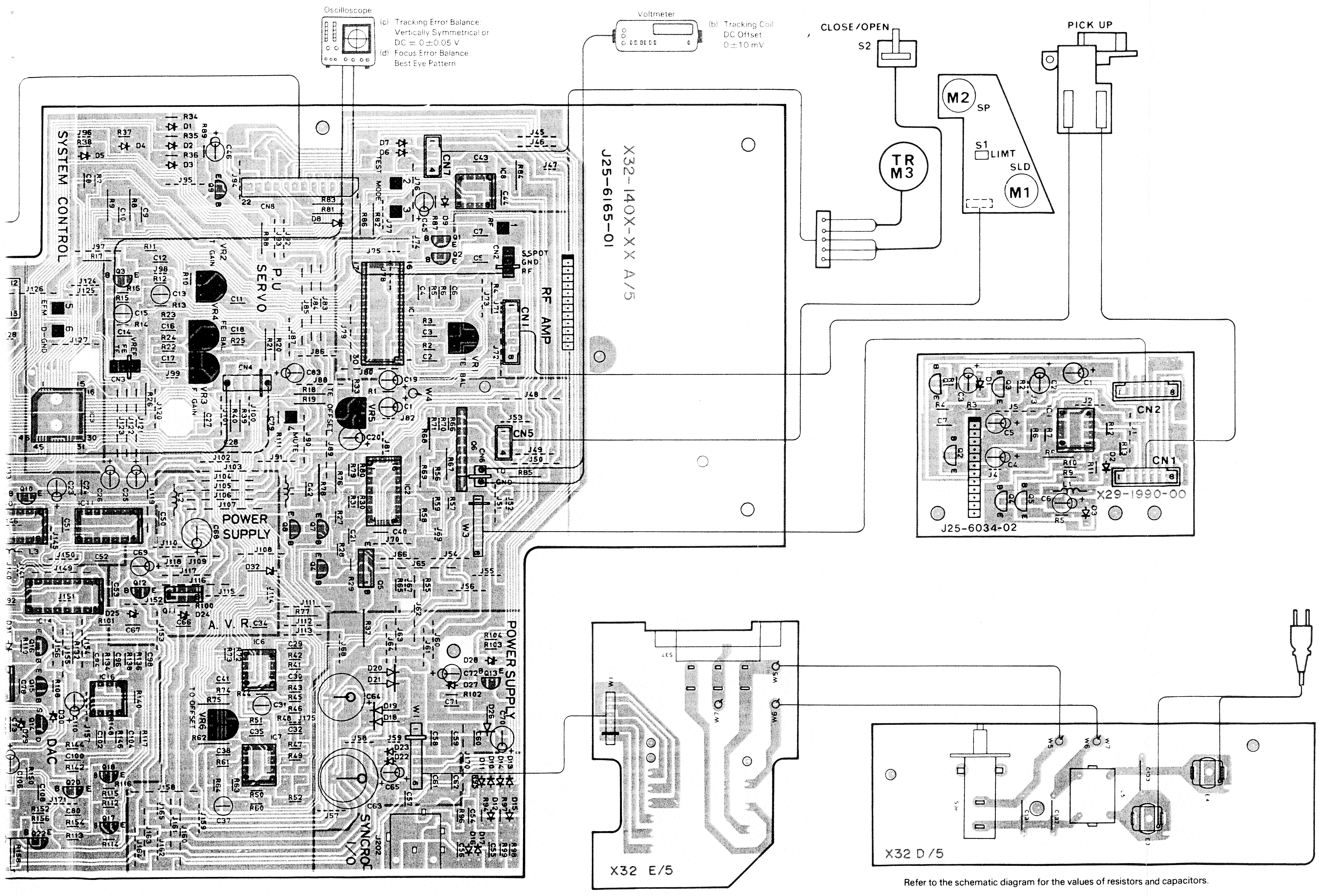
(d) Focus Error Balance Adjustment



(Picture 6) (0.5μsec/div)

- RF Signal during Test Mode (Play)
- Should be adjusted so that each center cross point will be a point, and so that points that cross above and below are clear, as shown in the picture. **(Picture 6)**


A
B
C
D
E
1
2
3
4
5
6
7
HEAD PHONE
X32 C/5 AMP
SYSTEM CONTROL
μ-COM
EFM DEC
DAC
X32B/5
FRONT



Refer to the schematic diagram for the values of resistors and capacitors.

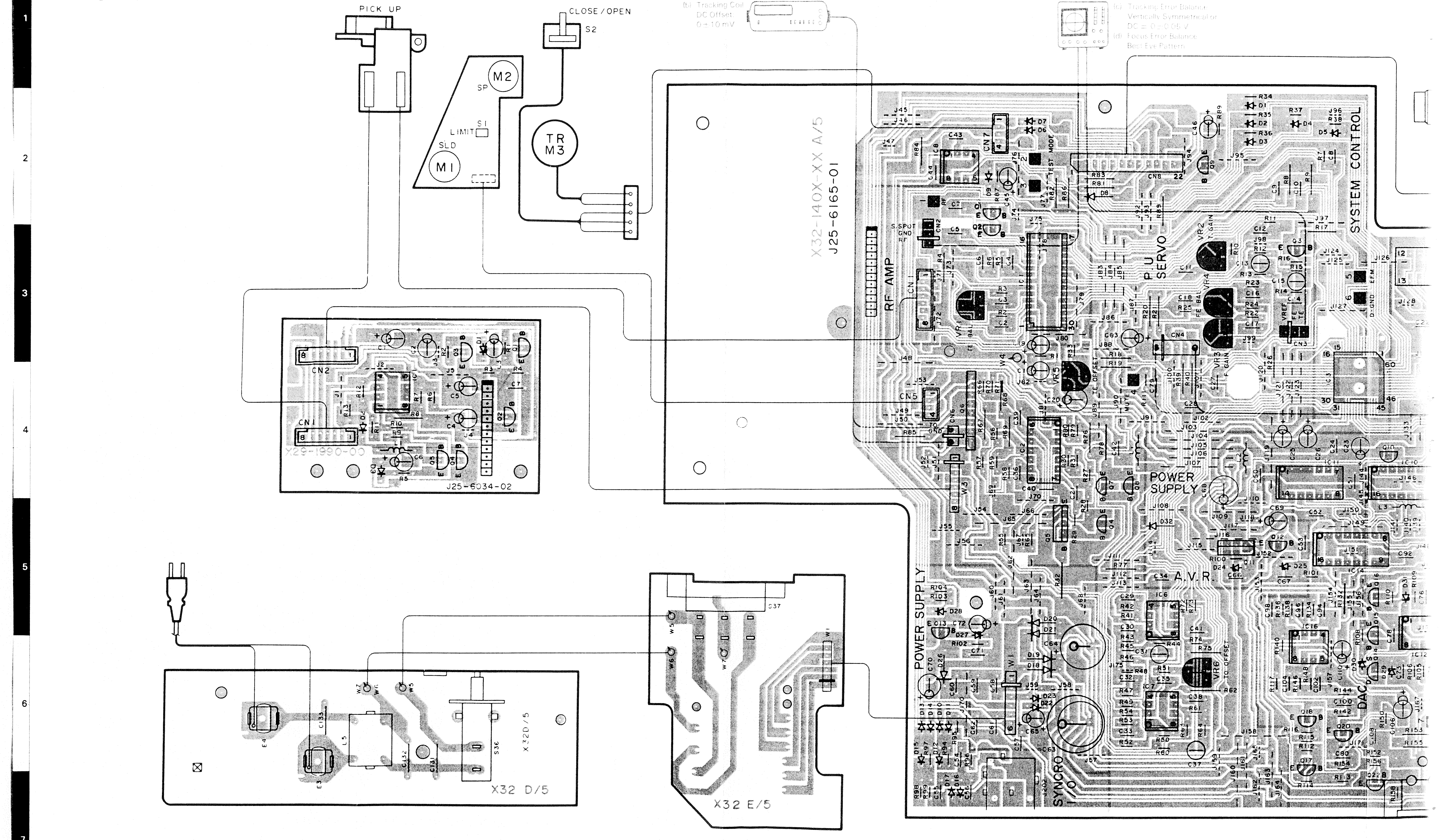
X29-1900-00

Ref. No. IC	Ref. No. Q	Address
	1	3K
	2	4L
	3	3L
	4	4L
	5	4L
1		4L

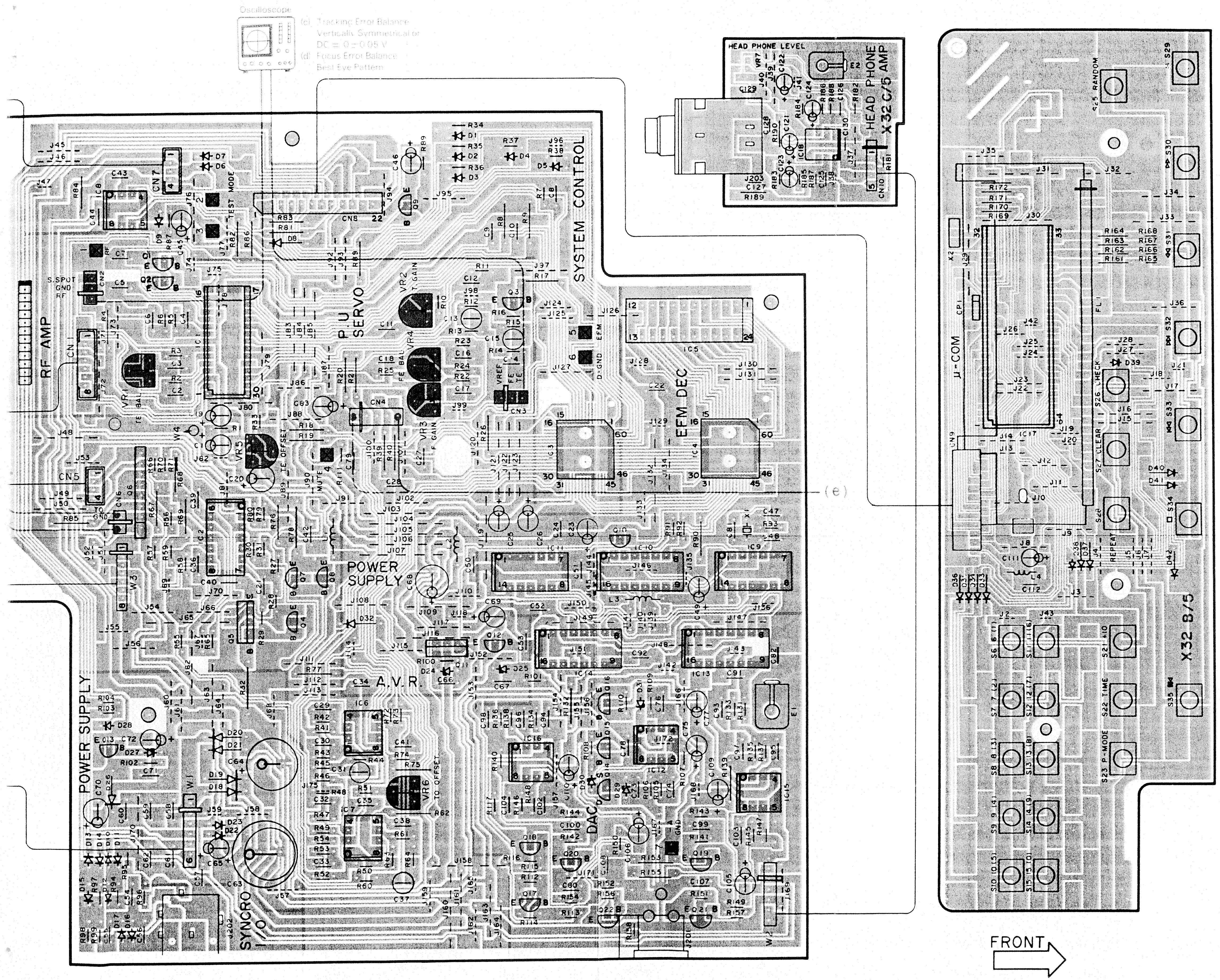
X32-1400-10

Ref. No. IC	Ref. No. Q	Address
	1	2H
	2	3H
	3	3F
	4	5G
	5	5H
	6	4H
	7	4G
	8	4G
	9	2F
	10	4E
	11	5F
	12	5F
	13	6H
	14	6E
	15	6E
	16	5E
	17	7F
	18	6F
	19	6E
	20	6F
	21	7E
	22	7E
1		3H
2		4H
3		4E
4		4D
5		3E
6		6G
7		6G
8		2H
9		4D
10		4E
11		4F
12		6E
13		5D
14		5E
15		6D
16		6F
17		3B
18		2D

PC BOARD (Foil Side View)



V W X Y Z AA AB AC AD



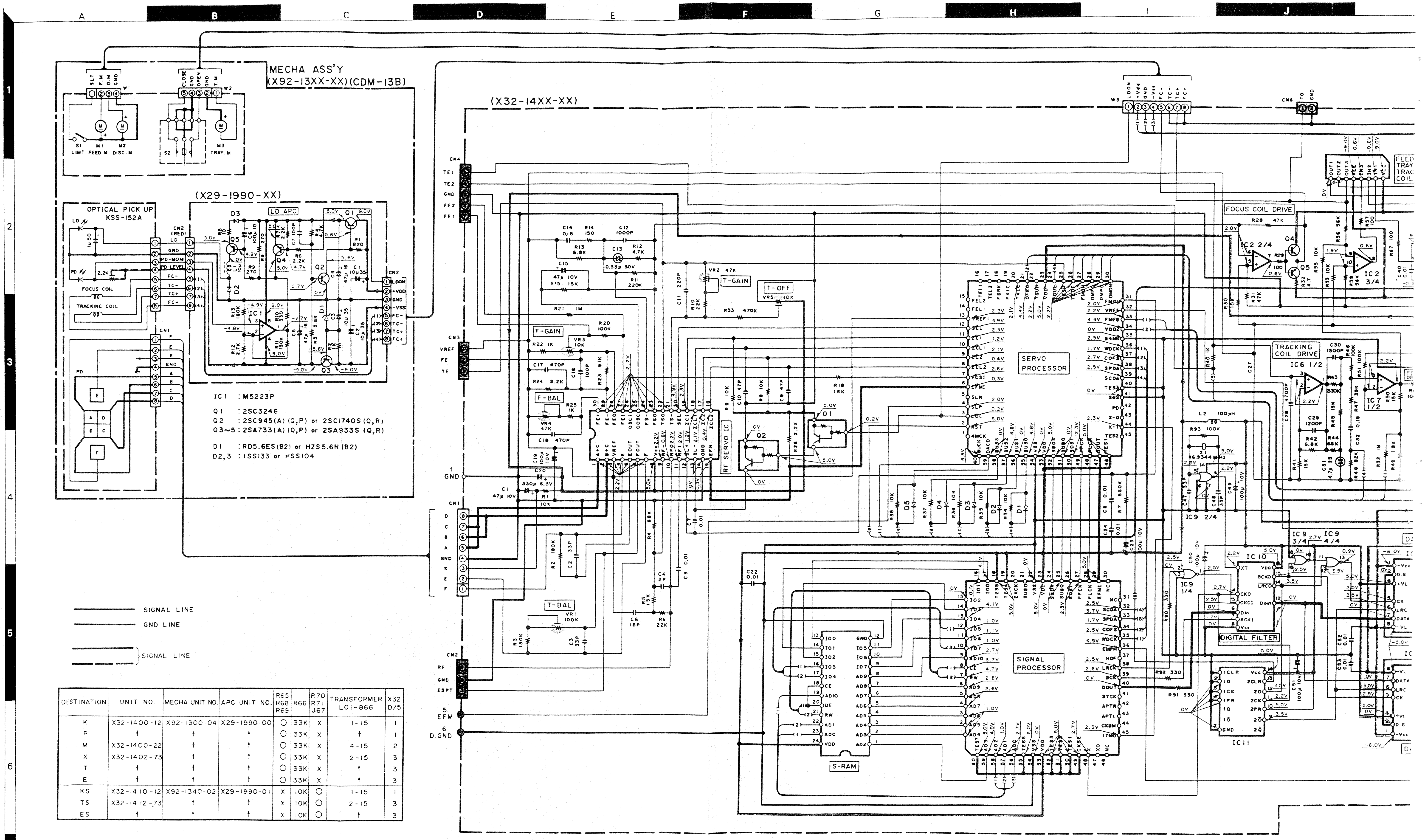
Refer to the schematic diagram for the values of resistors and capacitors.

X29-1900-00

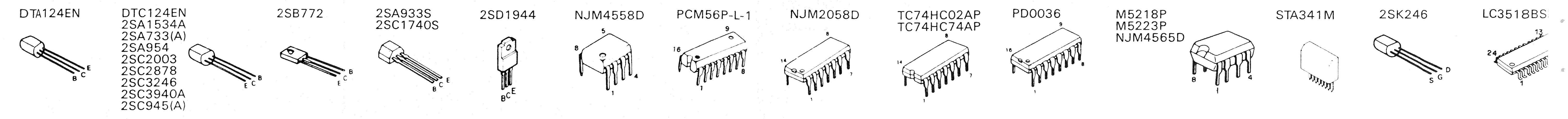
Ref. No. IC	Ref. No. Q	Address
	1	
	2	
	3	
	4	
	5	
1		

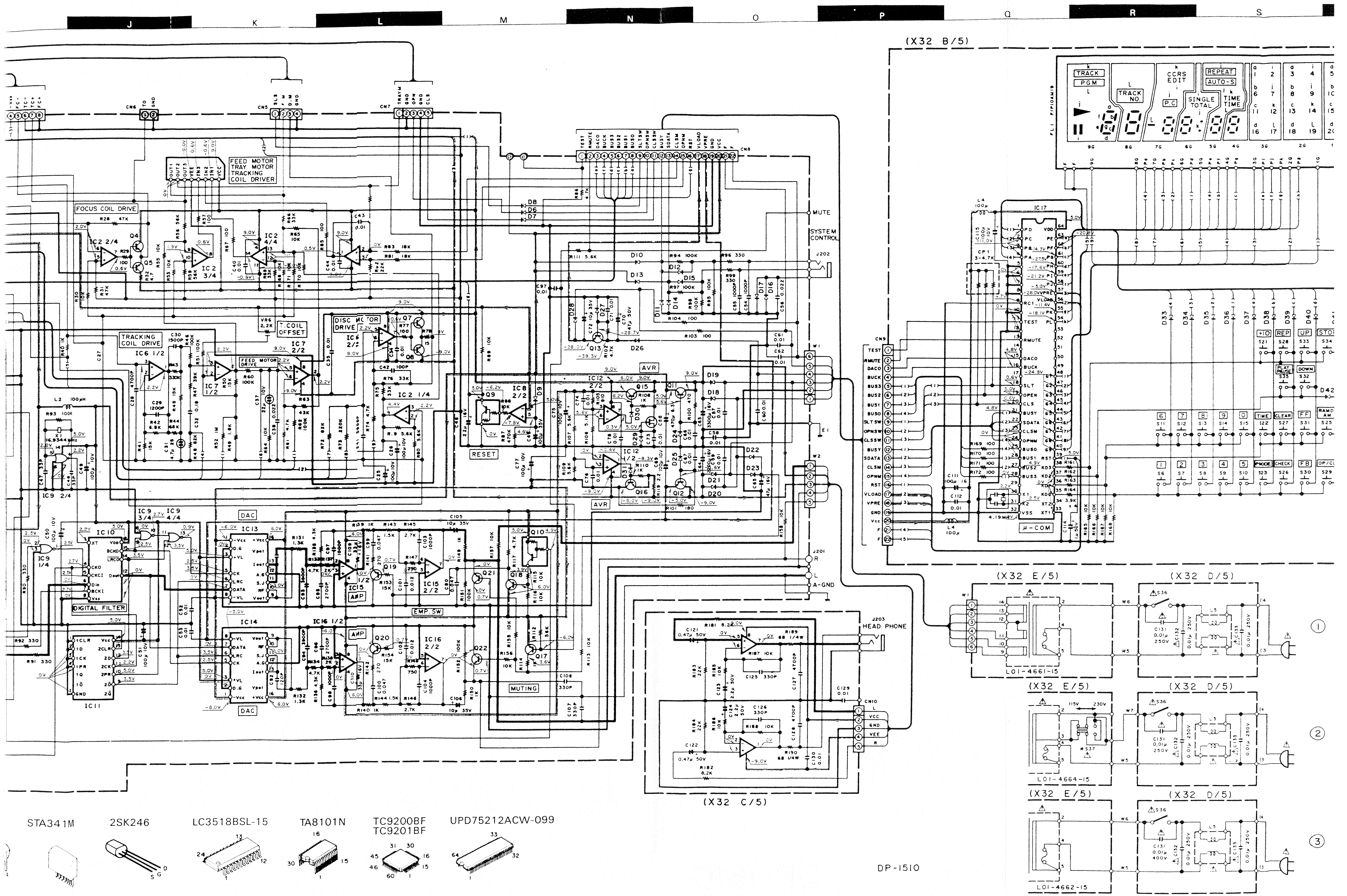
X32-1400-10

Ref. No. IC	Ref. No. Q	Address
	1	2W
	2	3W
	3	3Y
	4	5W
	5	5W
	6	4W
	7	4X
	8	4X
	9	2X
	10	
	11	5Y
	12	5Y
	13	5V
	14	6Z
	15	5Y
	16	5Y
	17	6Y
	18	6Y
	19	6Z
	20	6Y
	21	6Z
	22	6Z
1		3W
2		4W
3		4Y
4		4Z
5		3Z
6		5X
7		6X
8		2V
9		4AA
10		4Z
11		4Y
12		6Z
13		5Z
14		5Y
15		6Z
16		5Y
17		3AB
18		2AA

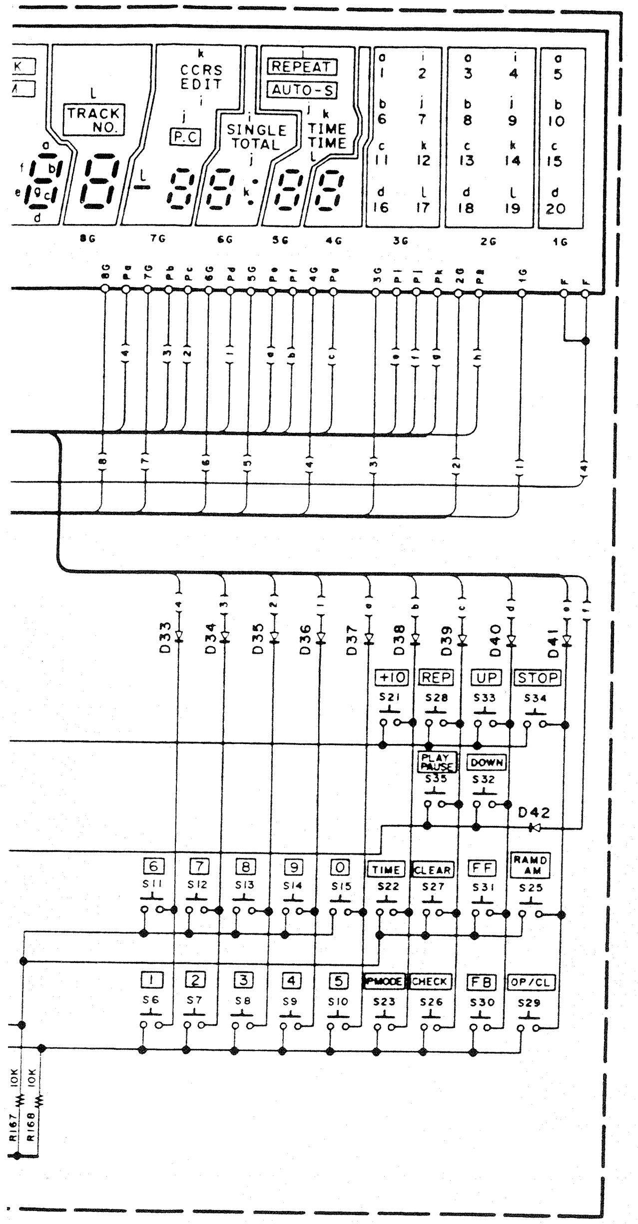


DESTINATION	UNIT NO.	MECHA UNIT NO.	APC UNIT NO.	R65 R68 R69	R66	R70 R71 J67	TRANSFORMER L01-866	X32 D/5
K	X32-1400-12	X92-1300-04	X29-1990-00	○	33K	X	1-15	1
P	↑	↑	↑	○	33K	X	↑	1
M	X32-1400-22	↑	↑	○	33K	X	4-15	2
X	X32-1402-73	↑	↑	○	33K	X	2-15	3
T	↑	↑	↑	○	33K	X	↑	3
E	↑	↑	↑	○	33K	X	↑	3
KS	X32-1410-12	X92-1340-02	X29-1990-01	X	10K	○	1-15	1
TS	X32-1412-73	↑	↑	X	10K	○	2-15	3
ES	↑	↑	↑	X	10K	○	↑	3





J K L M N O P Q R S
(X32 B/5)
FOCUS COIL DRIVE
FEED MOTOR TRAY MOTOR TRACKING COIL DRIVER
TRACKING COIL DRIVE
T.COIL OFFSET
DISC MOTOR DRIVE
FEED MOTOR DRIVE
RESET
AVR
MUTE
SYSTEM CONTROL
DAC
DIGITAL FILTER
AMP
EMP. SW
MUTING
HEAD PHONE
A-GND
μ-COM
TRACK
PGM
TRACK NO.
CCRS EDIT
P.C
SINGLE TOTAL
REPEAT
AUTO-S
TIME TIME
+10 REP UP STOP
PLAY PAUSE DOWN
TIME CLEAR FF
MODE CHECK FB
(X32 E/5)
(X32 D/5)
(X32 C/5)
L01-4661-15
L01-4664-15
L01-4662-15
STA341M
2SK246
LC3518BSL-15
TA8101N
TC9200BF
TC9201BF
UPD75212ACW-099
DP-1510



CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

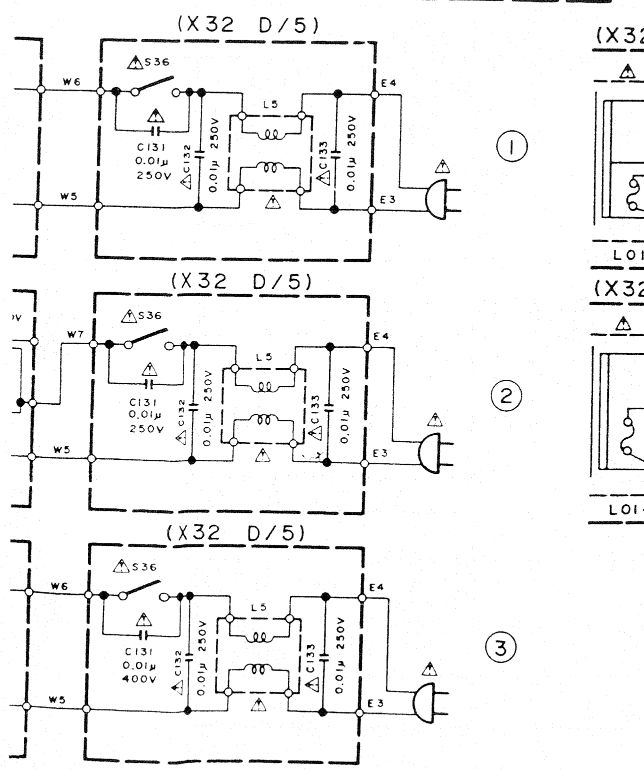
DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

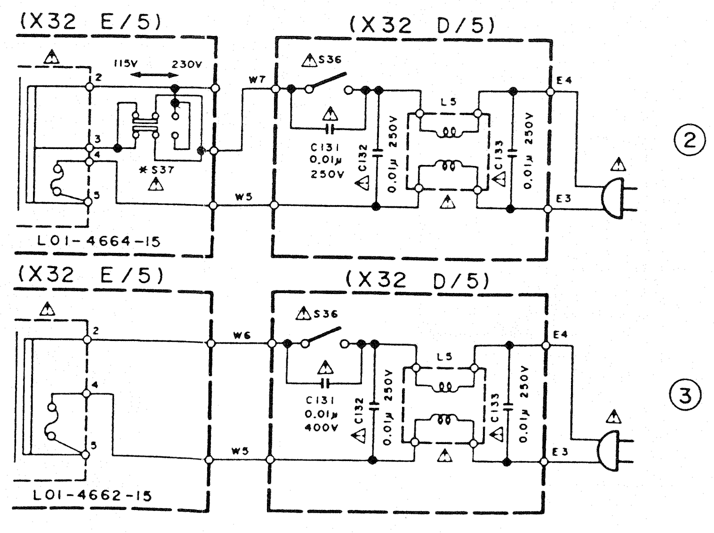
Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u. U. geringfügig.

(X32-1400-01)

IC1	:TA8101N
IC2	:NJM2058D
IC3	:TC9201BF
IC4	:TC9200BF
IC5	:HM6116ASP-15 or LC3518BSL-15
IC6～8,12	:NJM4558D
IC9	:TC74HC02AP
IC10	:PD0036
IC11	:TC74HC74AP
IC13,14	:PCM56P-L-1
IC15, 16	:NJM4565D
IC17	:μPD7521ZACW-099
IC18	:M5218P
Q1,10	:DTA124EN
Q2, 9	:DTC124EN
Q4, 7	:2SC3940A
Q5	:2SB772(Q, P)
Q6	:STA341M
Q8	:2SA1534A
Q11	:2SD1944
Q12, 13, 15	:2SA954(L, K)
Q14	:2SK246(Y, GR)
Q16	:2SC2003(L, K)
Q18, 18	:2SC1740S(Q, R) or 2SC945(A)(Q, P)
Q19～22	:2SC2878(B)
D1～17, 22, 23, 33～41	:HSS104 or ISS133
D18～21, 26	:S55 66B
D24, 25, 28	:HZS5.6N(B2) or RD5.6ES(B2)
D27	:HZS30N(B2) or RD30ES(B2)
D29	:HZS5.1N(B2) or RD5.1ES(B2)
D30～32	:HZS8.2N(B2) or RD8.2ES(B2)





DP-1510

KENWOOD

Y22-1670-11

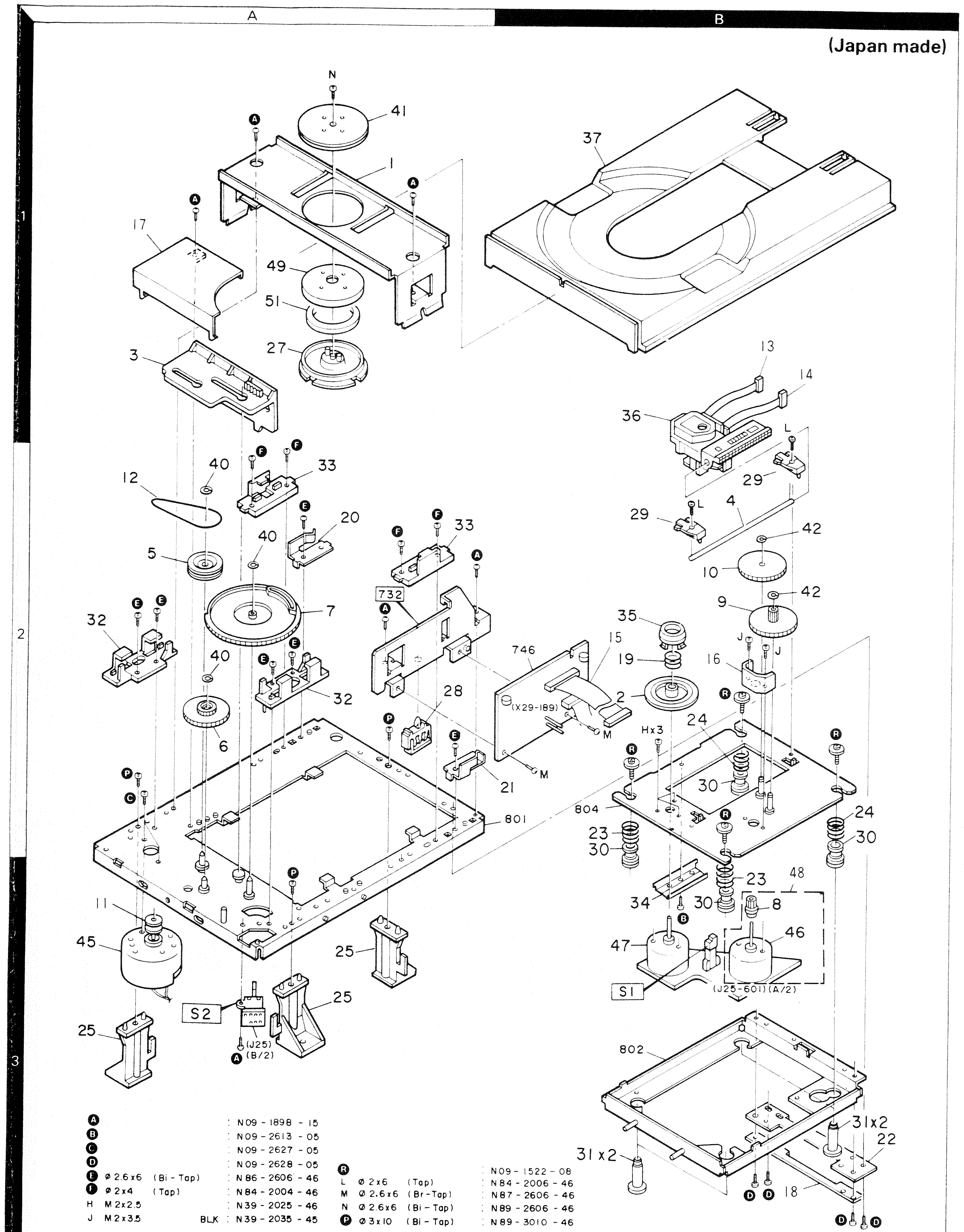
EXPLODED VIEW (MECHANISM)

DP-1510

(Japan made)

JAPAN MADE

SINGAPORE MADE

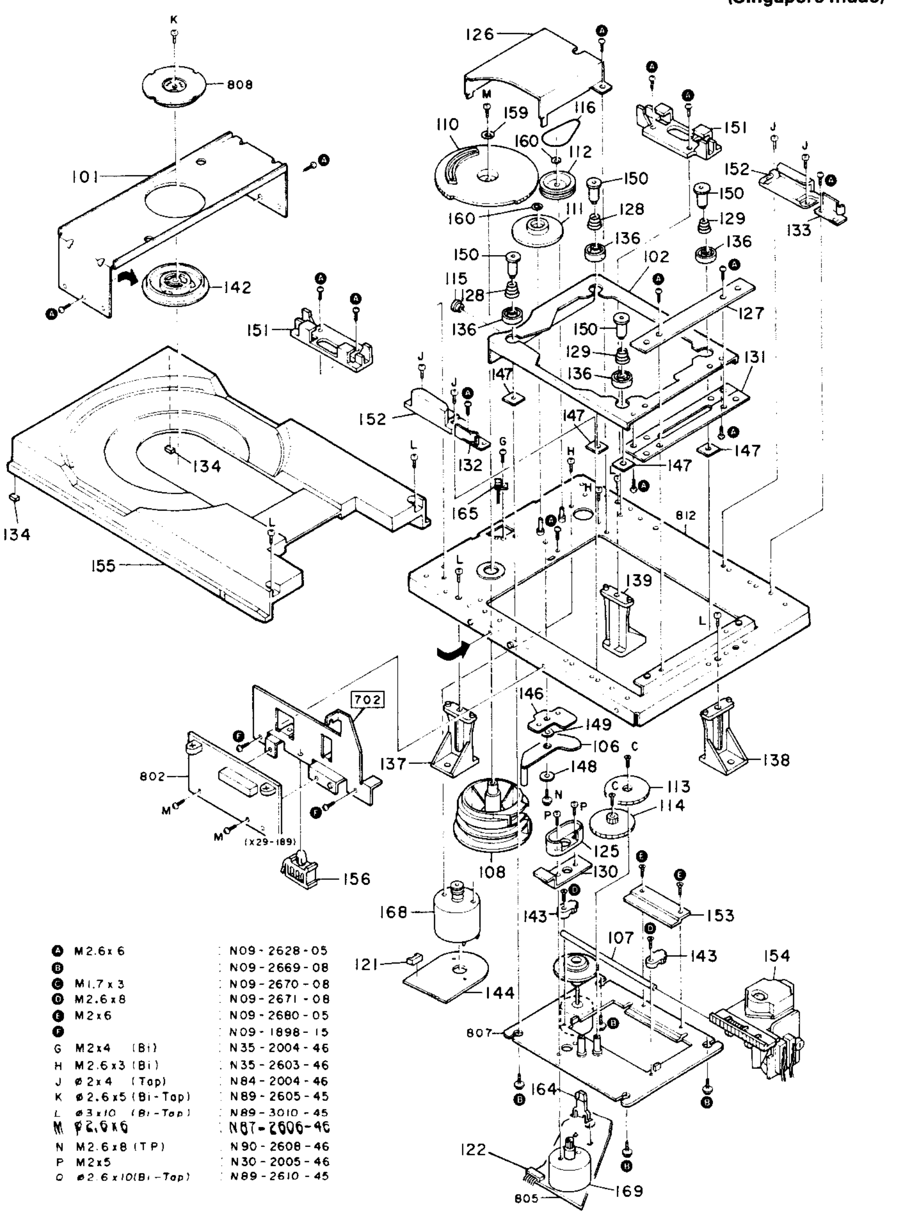


A			: N09-1898-15
B			: N09-2613-05
C			: N09-2627-05
D			: N09-2628-05
E	ø2.6x6	(Bi-Tap)	: N86-2606-46
F	ø2x4	(Tap)	: N84-2004-46
H	M2x2.5		: N39-2025-46
J	M2x3.5	BLK	: N39-2035-45
R			: N09-1522-08
L	ø2x6	(Tap)	: N84-2006-46
M	ø2.6x6	(Br-Tap)	: N87-2606-46
N	ø2.6x6	(Bi-Tap)	: N89-2606-46
P	ø3x10	(Bi-Tap)	: N89-3010-46

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (MECHANISM)

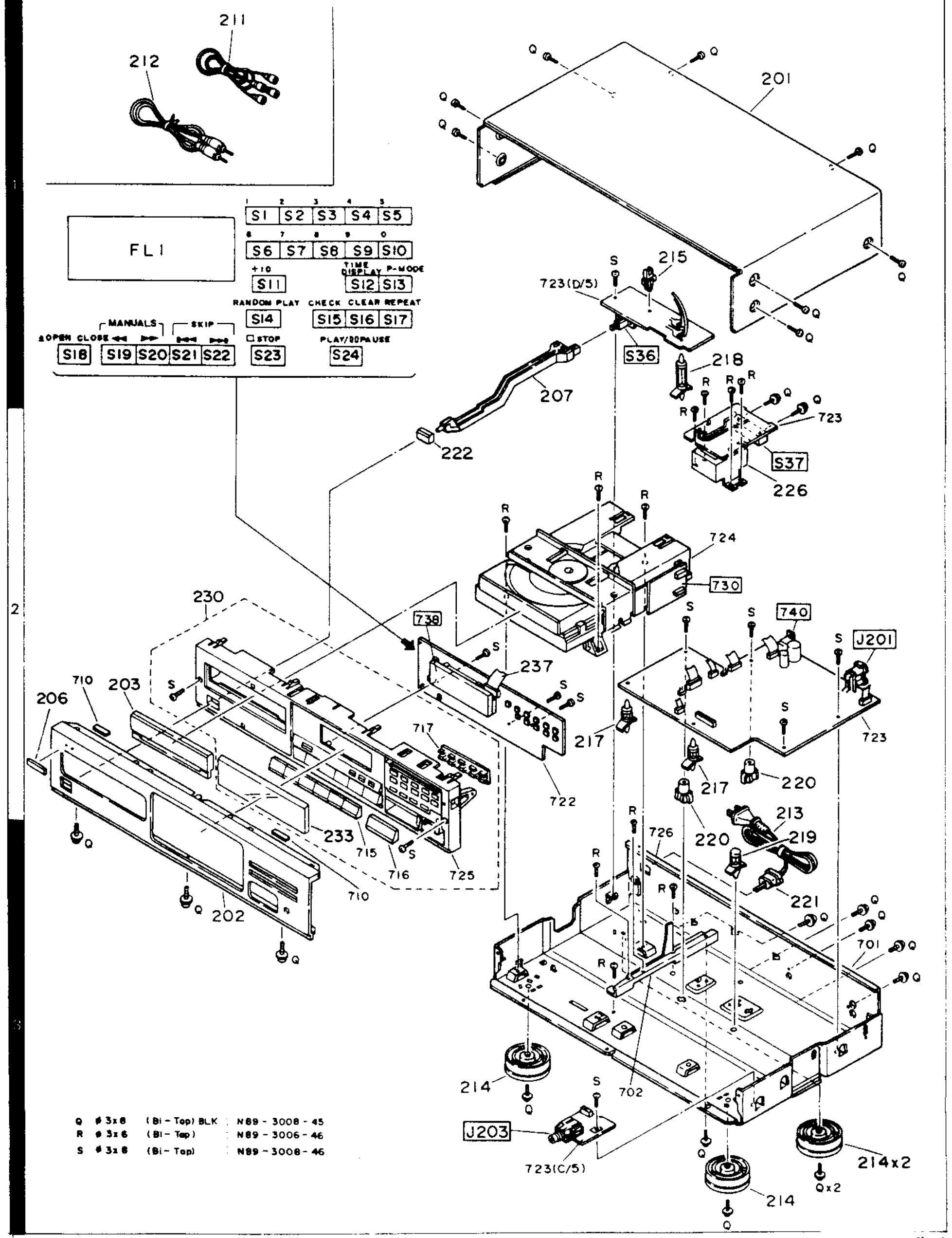
(Singapore made)



A	M2.6x6	N09-2628-05
B		N09-2669-08
C	M1.7x3	N09-2670-08
D	M2.6x8	N09-2671-08
E	M2x6	N09-2680-05
F		N09-1898-15
G	M2x4 (Bi)	N35-2004-46
H	M2.6x3 (Bi)	N35-2603-46
J	ø2x4 (Top)	N84-2004-46
K	ø2.6x5 (Bi-Top)	N89-2605-45
L	ø3x10 (Bi-Top)	N89-3010-45
M	ø2.6x6	N87-2606-46
N	M2.6x8 (TP)	N90-2608-46
P	M2x5	N30-2005-46
Q	ø2.6x10 (Bi-Top)	N89-2610-45

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



Q	ø3x8	(Bi-Top) BLK	N89-3008-45
R	ø3x6	(Bi-Top)	N89-3006-46
S	ø3x8	(Bi-Top)	N89-3008-46

Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

⁎ New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

⁎ 新規部品
(注)部品番号がないものは修理用部品として扱いません。

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
DP-1510						
201	1F		A01-1749-01	METALLIC CABINET		
201	1F		A01-1758-01	METALLIC CABINET		S
202	3E	⁎	A20-5816-02	PANEL		
203	2E		A29-0146-03	PANEL		
230	2E	⁎	A22-1094-03	SUB PANEL ASSY		
206	2E		B43-0287-04	KENWOOD BADGE		
233	2E	⁎	B03-2529-04	DRESSING PLATE		
-			B46-0092-03	WARRANTY CARD	K	
-			B46-0096-13	WARRANTY CARD	X	J
-			B46-0121-03	WARRANTY CARD	P	J
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-03	WARRANTY CARD	T	
-			B50-9502-00	INSTRUCTION MANUAL(ENGLISH)		J
-			B50-9503-00	INSTRUCTION MANUAL(FRENCH)	PME	J
-			B50-9504-00	INSTRUCTION MANUAL(S,A,C)	M	J
-			B50-9505-00	INSTRUCTION MANUAL(G,D,I)	E	J
-			B50-9555-00	INSTRUCTION MANUAL(ENGLISH)		S
-			B50-9556-00	INSTRUCTION MANUAL(FRENCH)	E	S
-			B50-9558-00	INSTRUCTION MANUAL(G,D,I)	E	S
207	1F		D21-1540-03	EXTENSION SHAFT		
211	1E		E30-0505-05	AUDIO CORD		
212	1E		E30-1392-05	CORD WITH PLUG	K	S
212	1E		E30-1392-05	CORD WITH PLUG	KPMX	J
213	2F		E30-2275-05	AC POWER CORD	X	J
⚠ 213	2F		E30-2276-05	AC POWER CORD	T	
⚠ 213	2F		E30-2277-05	AC POWER CORD	E	
213	2F		E30-2284-05	AC POWER CORD	M	J
213	2F		E30-2423-05	AC POWER CORD	K	S
213	2F		E30-2423-05	AC POWER CORD	KP	J
237	2F		E31-7045-05	FLAT CABLE(22P)		
-		⁎	H01-8477-04	ITEM CARTON CASE		J
-		⁎	H01-8480-04	ITEM CARTON CASE		S
-			H10-3801-12	POLYSTYRENE FOAMED FIXTURE		J
-			H10-3802-12	POLYSTYRENE FOAMED FIXTURE		J
-			H10-3817-02	POLYSTYRENE FOAMED FIXTURE		S
-			H10-3818-02	POLYSTYRENE FOAMED FIXTURE		S
-			H20-0554-04	PROTECTION COVER	M	J
-			H21-0264-04	PROTECTION SHEET		S
-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
-			H25-0330-04	PROTECTION BAG		S
-			H25-0330-04	PROTECTION BAG	KPXTE	J
214	3E,3F		J02-1034-05	FOOT		
215	1F		J11-0129-05	WIRE CLAMPER		
217	2F		J19-0515-05	UNIT HOLDER		
218	1F		J19-0581-05	UNIT HOLDER		
219	3F		J19-2536-05	UNIT HOLDER		
220	2F		J19-3180-05	UNIT HOLDER		
221	3F		J42-0083-05	POWER CORD BUSHING		S
221	3F		J42-0083-05	POWER CORD BUSHING	KP	J
221	3F		J42-0166-05	POWER CORD BUSHING	MXTE	J
222	2E		K27-1965-04	KNOB (BUTTON)		

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226	2F		L01-8661-15	POWER TRANSFORMER	K	S
226	2F		L01-8661-15	POWER TRANSFORMER	KP	J
226	2F		L01-8662-05	POWER TRANSFORMER	TE	S
226	2F		L01-8662-05	POWER TRANSFORMER	XTE	J
226	2F		L01-8664-05	POWER TRANSFORMER	M	J
Q			N89-3008-45	BINDING HEAD TAPTITE SCREW		
R			N89-3006-46	BINDING HEAD TAPTITE SCREW		
S			N89-3008-46	BINDING HEAD TAPTITE SCREW		
APC UNIT (X29-1990-00)						
C1 -3			CE04KW1V100M	ELECTRO 10UF 35WV		J
C1 -3			CE04LW1V100M	ELECTRO 10UF 35WV		S
C4 ,5			CE04KW1C470M	ELECTRO 47UF 16WV		J
C4 ,5			CE04LW1C470M	ELECTRO 47UF 16WV		S
C6			CE04KW1A101M	ELECTRO 100UF 10WV		J
C6			CE04LW1A101M	ELECTRO 100UF 10WV		S
C7			CC45FSL1H101J	CERAMIC 100PF J		
L1			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		
T			N87-2606-46	BRAZIER HEAD TAPTITE SCREW		
D1			HZS5.6N(B2)	ZENER DIODE		
D1			R05.6ES(B2)	ZENER DIODE		
D2 ,3			HSS104	DIODE		
D2 ,3			1SS133	DIODE		
IC1			M5223P	IC(OP AMP X2)		
Q1			2SC3246	TRANSISTOR		
Q2			2SC1740S(Q,R)	TRANSISTOR		
Q2			2SC945(A)(Q,P)	TRANSISTOR		
Q3 -5			2SA733(A)(Q,P)	TRANSISTOR		
Q3 -5			2SA933S(Q,R)	TRANSISTOR		
CD PLAYER UNIT (X32-1400-12: K, P, 0-22: M, 2-73: X, T, E)						
C1			CE04KW1A470M	ELECTRO 47UF 10WV		J
C1			CE04LW1A470M	ELECTRO 47UF 10WV		S
C2 ,3			CC45FSL1H330J	CERAMIC 33PF J		
C4			CC45FSL1H020C	CERAMIC 2.0PF C		
C5			CK45FF1H103Z	CERAMIC 0.010UF Z		
C6			CC45FSL1H180J	CERAMIC 18PF J		
C7 ,8			CK45FF1H103Z	CERAMIC 0.010UF Z		
C9 ,10			CC45FSL1H470J	CERAMIC 47PF J		
C11			CC45FSL1H221J	CERAMIC 220PF J		
C12			CF92FV1H102J	MF 1000PF J		
C13			C90-1398-05	NP-ELEC 0.33UF 50WV		
C14			CF92FV1H184J	MF 0.18UF J		J
C14			CF92FV1H474J	MF 0.47UF J		S
C15			CE04KW1A470M	ELECTRO 47UF 10WV		J
C15			C90-1333-05	NP-ELEC 22UF 10WV		S
C16			CC45FSL1H101J	CERAMIC 100PF J		
C17 ,18			CK45FB1H471K	CERAMIC 470PF K		
C19			CE04KW1A101M	ELECTRO 100UF 10WV		J
C19			CE04LW1A101M	ELECTRO 100UF 10WV		S
C20			CE04KW0J331M	ELECTRO 330UF 6.3WV		J
C20			CE04LW0J331M	ELECTRO 330UF 6.3WV		S
C22			CK45FF1H103Z	CERAMIC 0.010UF Z		
C23			CE04KW1A101M	ELECTRO 100UF 10WV		J
C23			CE04LW1A101M	ELECTRO 100UF 10WV		S

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C24			CK45FF1H103Z	CERAMIC 0.010UF Z		
C25 ,26			CE04KW1A101M	ELECTRO 100UF 10WV		J
C25 ,26			CE04LW1A101M	ELECTRO 100UF 10WV		S
C28			CF92FV1H472J	MF 4700PF J		
C29			CF92FV1H122J	MF 1200PF J		
C30			CF92FV1H152J	MF 1500PF J		
C31			C90-1352-05	NP-ELEC 4.7UF 25WV		
C32			CF92FV1H184J	MF 0.18UF J		
C34 ,35			CK45FF1H103Z	CERAMIC 0.010UF Z		
C37			C90-1333-05	NP-ELEC 22UF 10WV		
C38			CF92FV1H223J	MF 0.022UF J		
C40			CK45FF1H103Z	CERAMIC 0.010UF Z		
C41			CF92FV1H562J	MF 5600PF J		
C42			CC45FSL1H101J	CERAMIC 100PF J		
C43 ,44			CK45FF1H103Z	CERAMIC 0.010UF Z		
C45			CE04KW1V100M	ELECTRO 10UF 35WV		J
C45			CE04LW1V100M	ELECTRO 10UF 35WV		S
C46			CE04KW1C220M	ELECTRO 22UF 16WV		J
C46			CE04LW1C220M	ELECTRO 22UF 16WV		S
C47 ,48			CC45FCH1H330J	CERAMIC 33PF J		
C49			CE04LW1A101M	ELECTRO 100UF 10WV		S
C49 -51			CE04KW1A101M	ELECTRO 100UF 10WV		J
C50 -53			CK45FF1H103Z	CERAMIC 0.010UF Z		S
C52 ,53			CK45FF1H103Z	CERAMIC 0.010UF Z		J
C54 ,55			CK45FB1H102K	CERAMIC 1000PF K		
C56			CK45FF1H223Z	CERAMIC 0.022UF Z		J
C56 -62			CK45FF1H103Z	CERAMIC 0.010UF Z		S
C57 -62			CK45FF1H103Z	CERAMIC 0.010UF Z		J
C63			CE04KW1C332M	ELECTRO 3300UF 16WV		J
C63		⁎	CE04LW1C332M	ELECTRO 3300UF 16WV		S
C64			CE04KW1C222M	ELECTRO 2200UF 16WV		J
C64		⁎	CE04LW1C222M	ELECTRO 2200UF 16WV		S
C65			CE04KW1C470M	ELECTRO 47UF 16WV		J
C65			CE04LW1A470M	ELECTRO 47UF 10WV		S
C66 ,67			CK45FF1H103Z	CERAMIC 0.010UF Z		
C68			CE04KW0J471M	ELECTRO 470UF 6.3WV		J
C68			CE04LW0J471M	ELECTRO 470UF 6.3WV		S
C69			CE04KW1A101M	ELECTRO 100UF 10WV		J
C69			CE04LW1A101M	ELECTRO 100UF 10WV		S
C70			CE04KW1H470M	ELECTRO 47UF 50WV		J
C70			CE04LW1H470M	ELECTRO 47UF 50WV		S
C71			CK45FF1H103Z	CERAMIC 0.010UF Z		
C72			CE04KW1V100M	ELECTRO 10UF 35WV		J
C72			CE04LW1V100M	ELECTRO 10UF 35WV		S
C73 ,74			CK45FF1H103Z	CERAMIC 0.010UF Z		
C75			CE04KW1A101M	ELECTRO 100UF 10WV		J
C75			CE04LW1A101M	ELECTRO 100UF 10WV		S
C76			CK45FF1H103Z	CERAMIC 0.010UF Z		
C77			CE04KW1A101M	ELECTRO 100UF 10WV		J
C77			CE04LW1A101M	ELECTRO 100UF 10WV		S
C78			CK45FF1H103Z	CERAMIC 0.010UF Z		
C79			CF92FV1H103J	MF 0.010UF J		
C80			CF92FV1H473J	MF 0.047UF J		
C91 ,92			CF92FV1H121K	MF 120PF K		
C93 ,94			CF92FV1H392J	MF 3900PF J		

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C95 ,96			CF92FV1H272J	MF 2700PF J		
C97 ,98			CF92FV1H102J	MF 1000PF J		
C99 ,100			CF92FV1H473J	MF 0.047UF J		
C101,102			CF92FV1H123J	MF 0.012UF J		
C103,104			CF92FV1H102J	MF 1000PF J		
C105,106			CE04KW1V100M	ELECTRO 10UF 35WV		J
C105,106			CE04LW1V100M	ELECTRO 10UF 35WV		S
C107,108			CF92FV1H331K	MF 330PF K		J
C107,108			CK45FB1H331K	CERAMIC 330PF K		S
C109,110			CE04KW1E330M	ELECTRO 33UF 25WV		J
C109,110			CE04LW1E330M	ELECTRO 33UF 25WV		S
C111			CE04KW1A101M	ELECTRO 100UF 10WV		J
C111			CE04LW1A101M	ELECTRO 100UF 10WV		S
C112			CK45FF1H103Z	CERAMIC 0.010UF Z		
C121,122			CE04KW1HR47M	ELECTRO 0.47UF 50WV		J
C121,122			CE04LW1V100M	ELECTRO 10UF 35WV		S
C123,124			CE04KW1H2R2M	ELECTRO 2.2UF 50WV		J
C123,124			CE04LW1C220M	ELECTRO 22UF 16WV		S
C125,126			CK45FB1H331K	CERAMIC 330PF K		
C127,128			CK45FF1H472Z	CERAMIC 4700PF Z		
C129,130			CK45FF1H103Z	CERAMIC 0.010UF Z		
C131			C91-0647-05	CERAMIC 0.01UF P	XTE	J
C131-133			C91-0971-05	FILM 0.01UF 250WV		S
C131-133			C91-0971-05	FILM 0.01UF 250WV	KPM	J
C132,133			C91-0971-05	FILM 0.01UF 250WV	XTE	J
CN8			E10-2211-05	FLAT CABLE CONNECTOR		
CN9			E10-2212-05	FLAT CABLE CONNECTOR		
J201	2F		E13-0244-05	PHONO JACK		
J202			E11-0164-05	MINIATURE PHONE JACK(3P)		
J203	2F		E11-0162-05	PHONE JACK (3P)		
-			F29-0072-05	INSULATING COVER	XTE	J
-			J11-0098-05	WIRE CLAMPER		
-			J21-5159-04	MOUNTING HARDWARE	TE	S
-			J21-5159-04	MOUNTING HARDWARE	XTE	J
L1 -4			L40-1011-17	SMALL FIXED INDUCTOR(100UH,K)		S
L1 ,2			L40-1011-17	SMALL FIXED INDUCTOR(100UH,K)		J
L4			L40-1011-17	SMALL FIXED INDUCTOR(100UH,K)		J
⚠ L5		⁎	L79-0785-05	LINE FILTER		
X1			L77-1164-05	CRYSTAL RESONATOR		
X2			L78-0218-05	RESONATOR		
CP1		⁎	R90-0832-05	MULTIPLE RESISTOR		
R32			RS14KB3A4R7J	FL-PROOF RS 4.7 J 1W		
R78			RS14KB3A150J	FL-PROOF RS 15 J 1W		
VR1			R12-5058-05	TRIMMING POT.(100K)		
VR2			R12-3130-05	TRIMMING POT.(33K)		S
VR2			R12-3132-05	TRIMMING POT.(47K)		J
VR3			R12-3126-05	TRIMMING POT.(10K)		
VR4			R12-3130-05	TRIMMING POT.(33K)		
VR5			R12-3134-05	TRIMMING POT.(10K)		
VR6			R12-1100-05	TRIMMING POT.(2.2K)		
S6 -15			S40-1064-05	PUSH SWITCH		
S21 -23			S40-1064-05	PUSH SWITCH		
S25 -35			S40-1064-05	PUSH SWITCH		

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⚠ S36	1F		S40-1103-05	PUSH SWITCH (POWER TYPE)		
S37	1F		S31-2131-05	SLIDE SWITCH (POWER TYPE)	M	J
D1 -17			HSS104	DIODE		
D1 -17			1SS133	DIODE		
D18 -21			S5566B	DIODE		
D22 ,23			HSS104	DIODE		
D22 ,23			1SS133	DIODE		
D24 ,25			HZS5.6N(B2)	ZENER DIODE		
D24 ,25			RD5.6ES(B2)	ZENER DIODE		
D26			S5566B	DIODE		
D27			HZS30N(B)	ZENER DIODE		
D27			RD30ES(B)	ZENER DIODE		
D28			HZS5.6N(B2)	ZENER DIODE		
D28			RD5.6ES(B2)	ZENER DIODE		
D29			HZS5.1N(B2)	ZENER DIODE		
D29			RD5.1ES(B2)	ZENER DIODE		
D30 -32			HZS8.2N(B2)	ZENER DIODE		
D30 -32			RD8.2ES(B2)	ZENER DIODE		
D33 -42			HSS104	DIODE		
D33 -42			1SS133	DIODE		
FL1	1E		FIP10AM19	FLUORESCENT INDICATOR TUBE		
IC1			TA8101N	IC(SERVO)		
IC2			NJM2058D	IC(OP AMP X4)		
IC3			TC9201BF	IC(SERVO PROCESSOR)		
IC4			TC9200BF	IC(DATA PROCESSOR)		
IC5			LC3518BSL-15	IC(2KX8 RAM)		
IC6 -8			NJM4558D	IC(OP AMP X2)		
IC9			TC74HC02AP	IC(QUAD 2-INPUT NOR GATE)		
IC10			SM5807EP	IC(DIGITAL FILTER FOR CD)		
IC11			TC74HC74AP	IC(DUAL D-TYPE FLIP FLOP)		
IC12			NJM4558D	IC(OP AMP X2)		
IC13,14			PCM56P-L-1	IC(DA CONVERTER)		
IC15,16			NJM4565D	IC(OP AMP X2)		
IC17			UPD75212ACW-099	IC(MICROPROCESSOR)		
IC18			M5218P	IC(OP AMP X2)		
Q1			DTA124EN	DIGITAL TRANSISTOR		
Q2			DTC124EN	DIGITAL TRANSISTOR		
Q3			2SC1740S(Q,R)	TRANSISTOR		S
Q3			2SC945(A)(Q,P)	TRANSISTOR		S
Q4			2SC3940A	TRANSISTOR		
Q5			2SB772(Q,P)	TRANSISTOR		
Q6			STA341M	TRANSISTOR		
Q7			2SC3940A	TRANSISTOR		
Q8			2SA1534A	TRANSISTOR		
Q9			DTC124EN	DIGITAL TRANSISTOR		
Q10			DTA124EN	DIGITAL TRANSISTOR		
Q11			2SD1944	TRANSISTOR		
Q12 ,13			2SA954(L,K)	TRANSISTOR		
Q14			2SK246(Y,GR)	FET		
Q15			2SA954(L,K)	TRANSISTOR		
Q16			2SC2003(L,K)	TRANSISTOR		
Q17 ,18			2SC1740S(Q,R)	TRANSISTOR		
Q17 ,18			2SC945(A)(Q,P)	TRANSISTOR		
Q19 -22			2SC2878(B)	TRANSISTOR		

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JAPAN MADE

MECHANISM UNIT (X92-1300-04): Japan made

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1	1A		A11-0278-03	SUB CHASSIS		J
			D40-0837-05	MECHANISM ASSY		S
2	2B	⁎	D02-0086-08	TURNTABLE PLATTER		J
3	1A		D10-2227-03	SLIDER		J
4	2B	⁎	D10-2249-04	ROD		J
5	2A		D13-0722-04	GEAR		J
6	2A		D13-0723-04	GEAR		J
7	2A		D13-0724-03	GEAR		J
8	3B	⁎	D13-0745-08	GEAR		J
9	2B	⁎	D13-0746-08	GEAR		J
10	2B	⁎	D13-0747-14	GEAR		J
11	3A		D15-0284-04	MOTOR PULLEY		J
12	2A		D16-0191-04	BELT		J
13	1B	⁎	E31-4183-15	WIRING HARNESS		J
14	1B	⁎	E31-4845-05	WIRING HARNESS		
16	2B	⁎	F07-0546-08	COVER		J
17	1A	⁎	F19-0593-04	BLIND PLATE		J
18	3B	⁎	F31-0182-04	REINFORCING HARDWARE		J
19	2B	⁎	G01-2308-08	COMPRESSION SPRING		J
20	2A		G02-0493-04	FLAT SPRING		J
21	2B		G02-0494-04	FLAT SPRING		J
22	3B		G02-0495-08	FLAT SPRING		J
23	2B,3B	⁎	G01-2391-08	COMPRESSION SPRING		J
24	2B	⁎	G01-2392-08	COMPRESSION SPRING		J
25	3A		J02-0386-04	FOOT		J
27	1A		J11-0130-03	CLAMPER		J
28	2A		J11-0134-05	WIRE CLAMPER		
29	2B	⁎	J19-3165-03	HOLDER		J
30	2B,3B		J02-1027-05	INSULATOR		J
31	3B		J42-0170-08	BUSHING		J
32	2A	⁎	J90-0617-03	GUIDE		J
33	2A	⁎	J90-0618-03	GUIDE		J
34	3B	⁎	J90-0623-08	RAIL		J
35	2B	⁎	J90-0624-08	GUIDE		J
36	1B	⁎	J91-0393-05	PICKUP		J
37	1B		J99-0053-01	TRAY		J
-			J61-0081-05	WIRE BAND		S
40	2A		N19-0891-04	FLAT WASHER		J
41	1A		N19-1170-04	FLAT WASHER		J
42	2B	⁎	N19-1179-05	FLAT WASHER		J
A	2A		N09-1898-15	MACHINE SCREW		
B	3B	⁎	N09-2613-05	SEMS (TAPTITE SCREW)		J
C	2A	⁎	N09-2627-05	MACHINE SCREW		J
D ,L	3B	⁎	N09-2680-05	MACHINE SCREW		J
E	2A	⁎	N09-2628-05	MACHINE SCREW		J
F	2A		N84-2004-46	PAN HEAD TIPTITE SCREW		J
H	2B		N39-2025-46	PAN HEAD MACHINE SCREW		J
J	2B		N39-2035-45	PAN HEAD MACHINE SCREW		J
N	1A		N89-2606-46	BINDING HEAD TAPTITE SCREW		J
P	3A		N89-3010-46	BINDING HEAD TAPTITE SCREW		J

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JAPAN MADE

SINGAPORE MADE

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R	2B		N09-1522-05	SET SCREW (3X8)		J
S1		✱	S46-1122-05	LEAF SWITCH		J
S2			S33-2060-05	LEVER ROTARY SWITCH		J
45	3A		T42-0483-05	DC MOTOR		J
46	3B	✱	T42-0495-05	DC MOTOR		J
47	3B	✱	T42-0496-05	DC MOTOR		J
48	3B	✱	T42-0497-08	MOTOR ASSY		J
49	1A		T50-1036-04	YOKE		J
51	1A		T99-0222-05	MAGNET		J
		✱	X29-1990-01	CONTROL CIRCUIT UNIT		S
MECHANISM ASS'Y (X92-1340-00) : Singapore made						
101	1C		A11-0617-08	SUB CHASSIS ASSY		
102	2D		A11-0618-08	SUB CHASSIS ASSY		
106	2D	✱	D10-2314-08	STOPPER LINK ASSY		
107	3D		D10-2315-08	ROD		
108	3D	✱	D12-0126-08	CONTROL CAM		
110	1C	✱	D13-0799-08	DRIVE GEAR		
111	1D	✱	D13-0800-08	GEAR		
112	1D	✱	D13-0801-08	LOADING PULLEY		
113	2D		D13-0802-08	GEAR (A)		
114	2D		D13-0803-08	GEAR (B)		
115	1D	✱	D14-0300-08	ROLLER		
116	1D	✱	D16-0276-08	BELT (M)		
121	3C		E40-3263-05	CONNECTOR (SP)		
122	3C,3D	✱	E40-3262-05	CONNECTOR		
125	3D		F07-0554-08	COVER (GEAR)		
126	1D	✱	F19-0595-08	COVER (GEAR)		
127	1D	✱	F31-0187-08	REINFORCING HARDWARE		
130	3D	✱	F31-0188-08	STOPPER		
128	1D	✱	G01-2375-08	COMPRESSION SPRING (A)		
129	1D	✱	G01-2376-08	COMPRESSION SPRING (B)		
131	1D	✱	G02-0917-08	SPRING		
132	2D	✱	G02-0918-08	TRAY GUIDE SPRING (R)		
133	1D	✱	G02-0919-08	TRAY GUIDE SPRING (L)		
134	2C	✱	G13-0237-08	CUSHION		
136	1D	✱	J02-1019-08	INSULATOR		
137	2C	✱	J02-1020-08	FOOT		
138	2D	✱	J02-1021-08	FOOT (REAR)		
139	2D	✱	J02-1022-08	FOOT (L)		
142	1C	✱	J11-0145-08	CLAMPER		

E: Scandinavia & Europe K: USA P: Canada
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UE: AAFES(Europe) X: Australia

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F: France made
⚠ indicates safety critical components.

PARTS LIST

SINGAPORE MADE

✱ New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
143	3D		J19-3148-08	HOLDER (ROD)		
144	3D	✱	J25-6134-08	PRINTED WIRING BOARD(MOTOR)		
146	2D	✱	J30-0261-08	SPACER		
147	2D	✱	J30-0262-08	SPACER		
148	2D	✱	J30-0263-08	SPACER		
149	2D	✱	J32-0828-08	BOSS		
150	1D	✱	J42-0619-08	BUSHING		
151	1C,1D	✱	J90-0638-08	GUIDE (FRONT)		
152	2C,1D	✱	J90-0639-08	GUIDE (REAR)		
153	3D		J90-0640-08	GUIDE (SLIDE)		
154	3D	✱	J91-0385-08	PICK UP		
[illegible]	2D	✱	J99-0064-08	TRAY		
156	3D		J11-0134-05	WIRE CLAMPER		
[illegible]	[illegible]		J61-0307-08	WIRE BAND		
[illegible]	1D	✱	N19-1208-08	FLAT WASHER		
160	1D	✱	N19-1209-08	FLAT WASHER		
[illegible]	1C,1D		N09-2628-05	SCREW		
[illegible]	3D	✱	N09-2669-08	SCREW		
[illegible]	2D		N09-2670-08	SCREW (M1.7X3)		
[illegible]	3D		N09-2671-08	SCREW		
[illegible]	3D		N09-2680-05	SCREW		
[illegible]	2D		N09-1898-[illegible]	MACHINE SCREW		
164	3D		S46-1128-08	LEAF SWITCH		
165	2D	✱	S46-2109-08	LEAF SWITCH		
168	3D	✱	T42-0526-08	MOTOR ASSY (LOADING)		
169	3D	✱	T42-0527-08	MOTOR ASSY (SLED)		

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DP-1510

SPECIFICATIONS

[Format]

Type: .... Compact disc player
Read system: .... Non-contact optical pickup
Rotational speed: .... About 200 to 500 rpm

[Audio]

	DP-3010	DP-2010	DP-1510
Frequency response:	10 Hz ~ 20 kHz ±1 dB	10 Hz ~ 20 kHz ±1 dB	10 Hz ~ 20 kHz ±1 dB
Signal-to-noise ratio:	more than 100 dB	more than 100 dB	more than 100 dB
Total harmonic distortion:	0.007% at 1 kHz	0.008% at 1 kHz	0.008% at 1 kHz
Channel separation:	more than 96 dB at 1 kHz	more than 96 dB at 1 kHz	more than 96 dB at 1 kHz
Wow flutter:	Below measurable limit	Below measurable limit	Below measurable limit
Output level/impedance			
Line output:	1.2 V/1 kΩ	1.2 V/1 kΩ	1.2 V/1 kΩ
Headphone:	31 mW/32 Ω	31 mW/32 Ω	31 mW/32 Ω

[General]

Power consumption: .... 12 W
Dimensions: .... W:440 mm (17-5/16")
H:108 mm (4-1/4")
D:262 mm (10-5/16")
Weight: .... 3.8 kg (8.4 lb)

Note:
KENWOOD follows a policy of continuous development. For this reason specifications may be changed without notice.

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